HCDC Chip Overview: configuration and control

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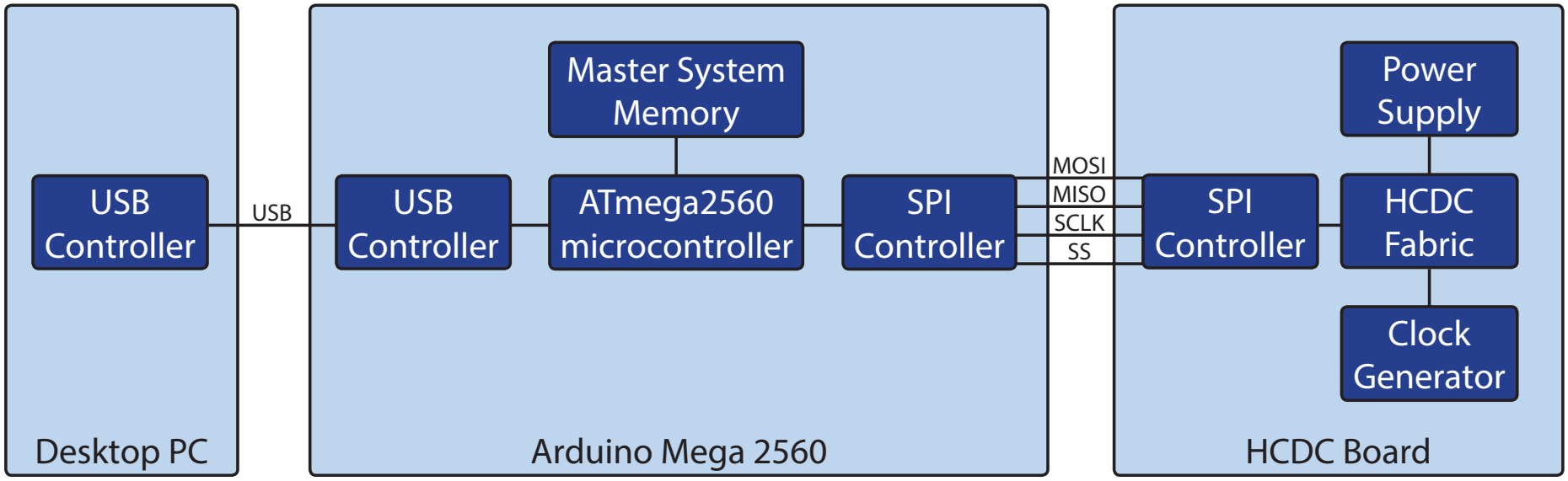
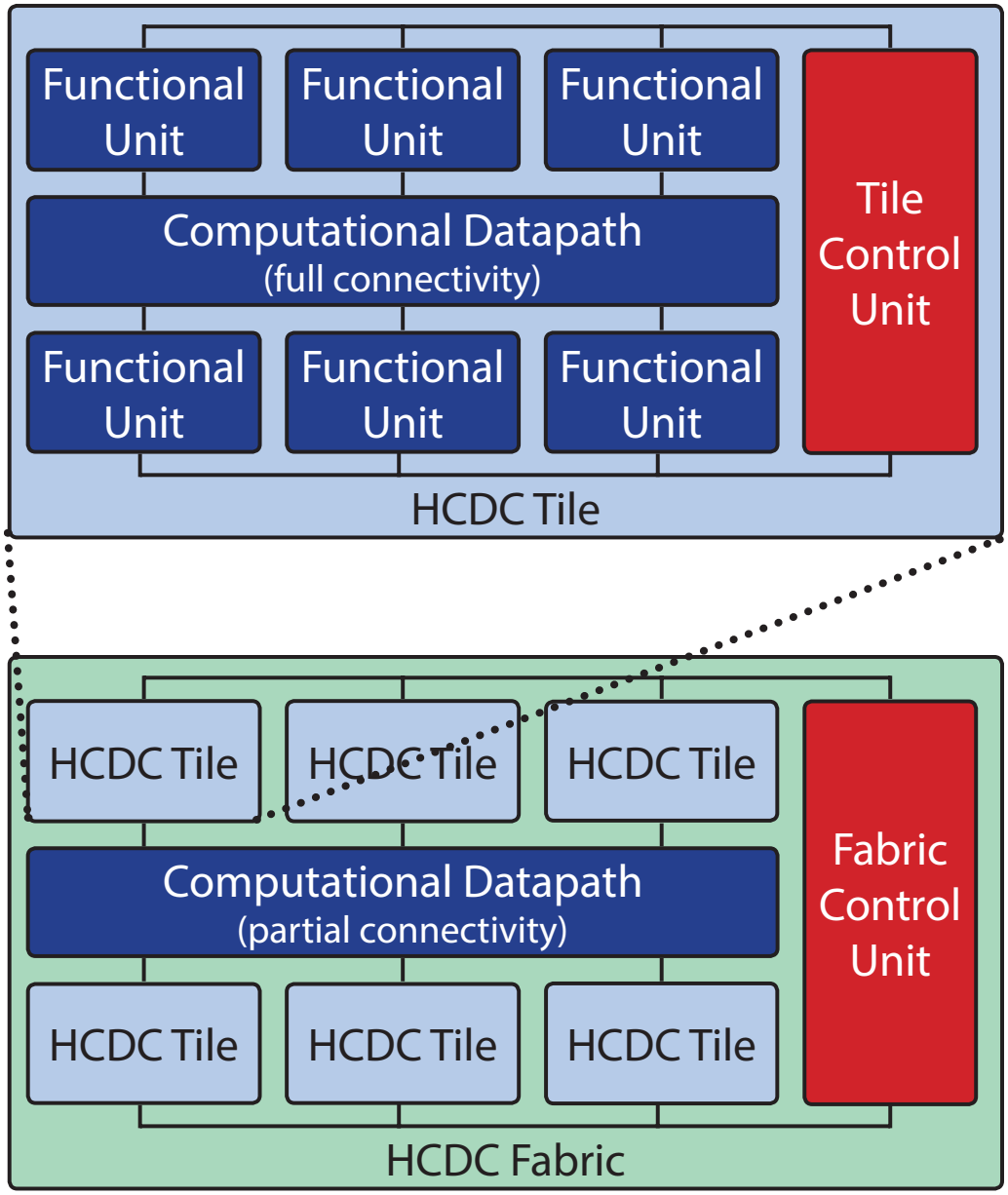
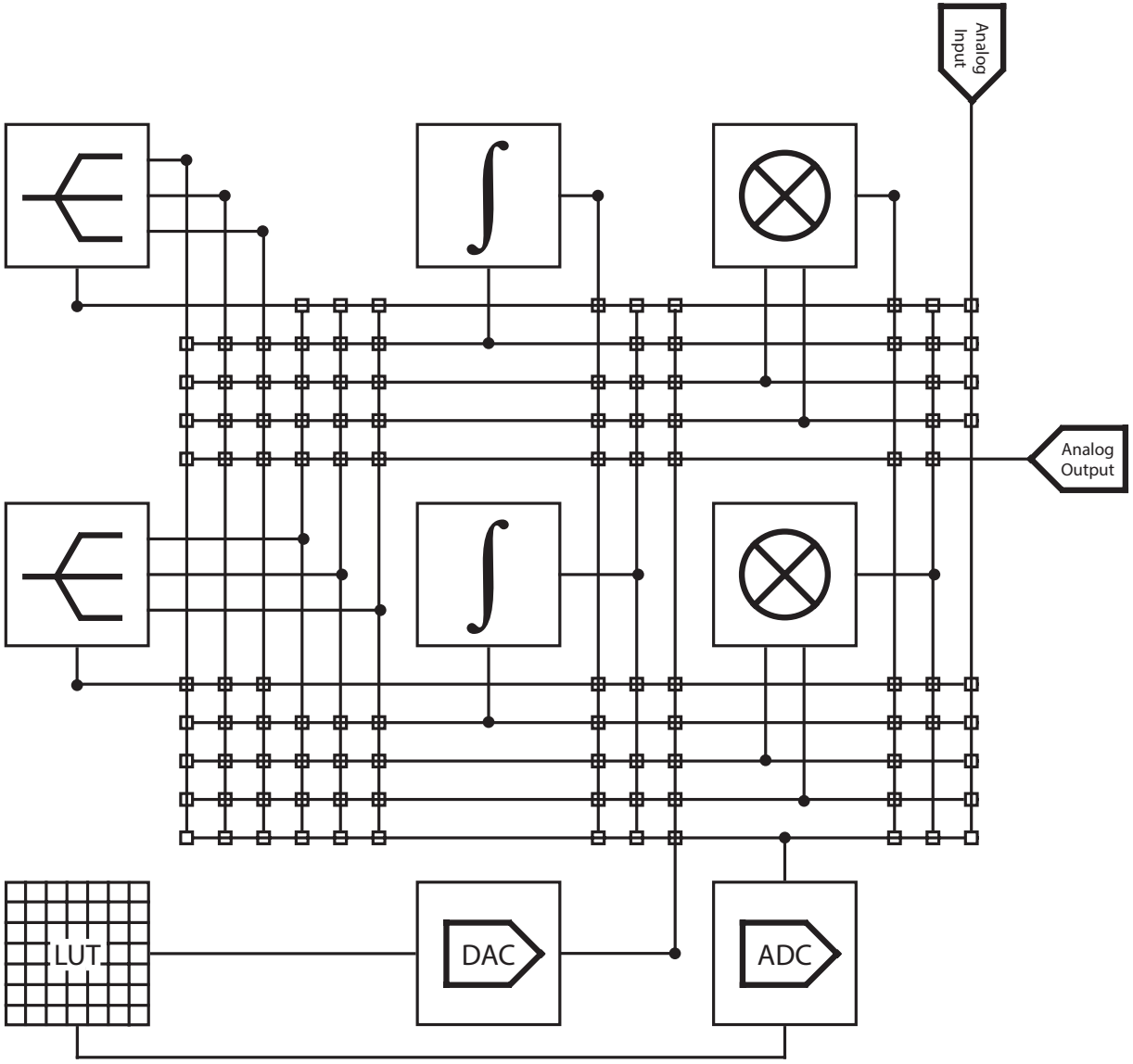
HCDC System Architecture



HCDC Chip Architecture



Chip Computational Datapath



Data Input Output Channels

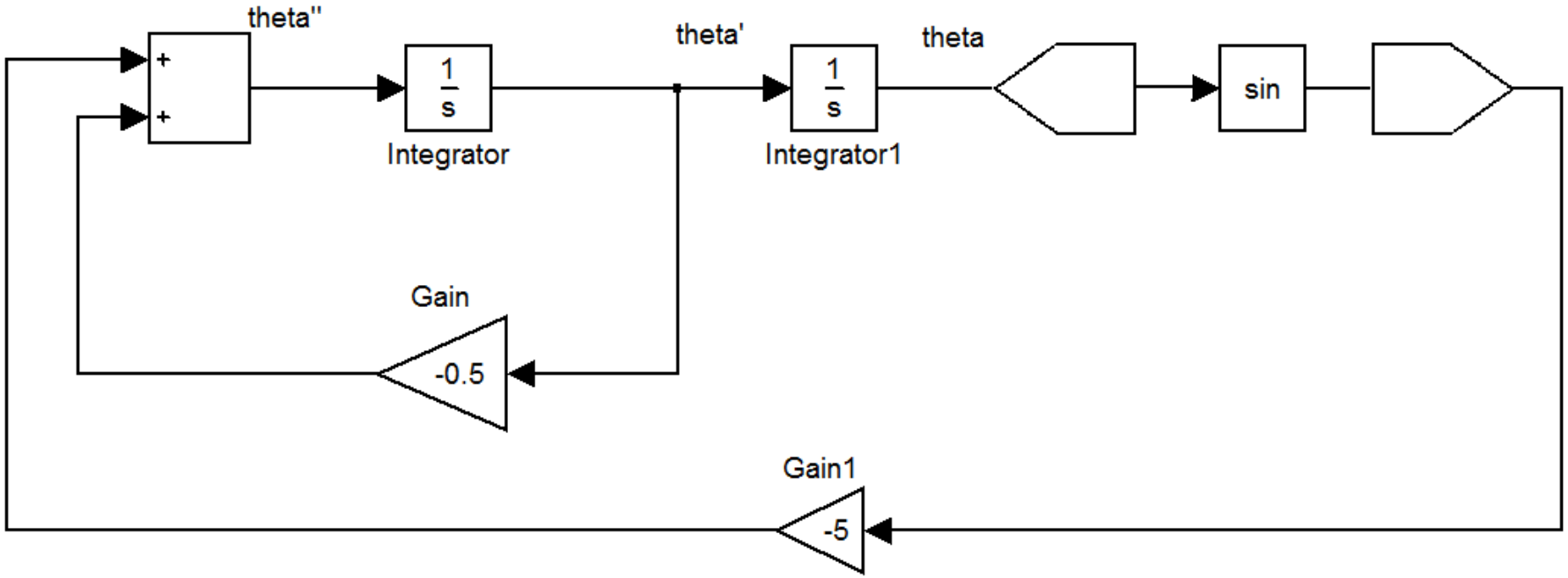
Channel Type	Number Available	Precision	Update Frequency
Analog simulation data input	4	Native	Native
Analog simulation data output	4	Native	Native
Digital initial condition input	4	8 bit	At simulation start
Digital simulation data parallel input	1	8 bit	As fast as ADC
Digital simulation data parallel output	1	8 bit	As fast as DAC
Digital simulation data serial output	2	8 bit	700 KHz

Phases of Operation

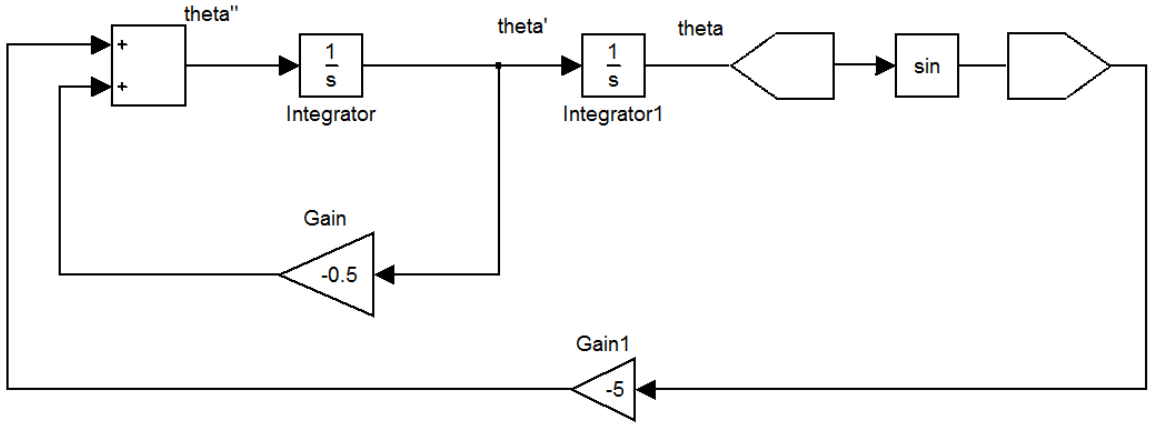
- CONFIGURATION of equation, coefficients, initial conditions
- CALIBRATION of electrical gain and offsets
- EXECUTION of circuit that simulates the desired equation
  - Indefinite operation
  - Timeout
- Gathering EXCEPTION information from completed simulation
  - Overflow (saturation)
  - Underflow (loss of precision)

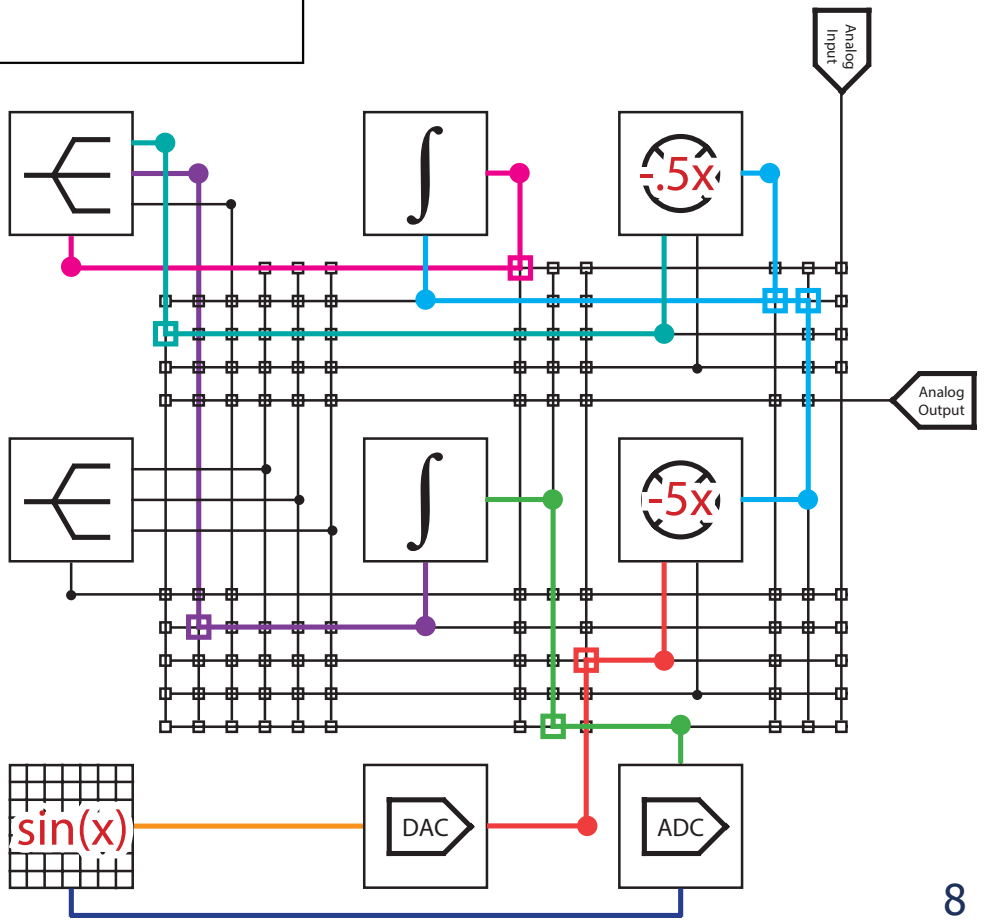
Example: Modeling an Equation

$$\ddot{\Theta} = -0.5 * \dot{\Theta} - 5*\sin\Theta, \Theta(0) = 1$$



Example: Mapping to Chip





Chip Configuration Protocol

- System master provides configuration via SPI interface
- Messages are 24 bits, sent over SPI

Example: Configuration Message

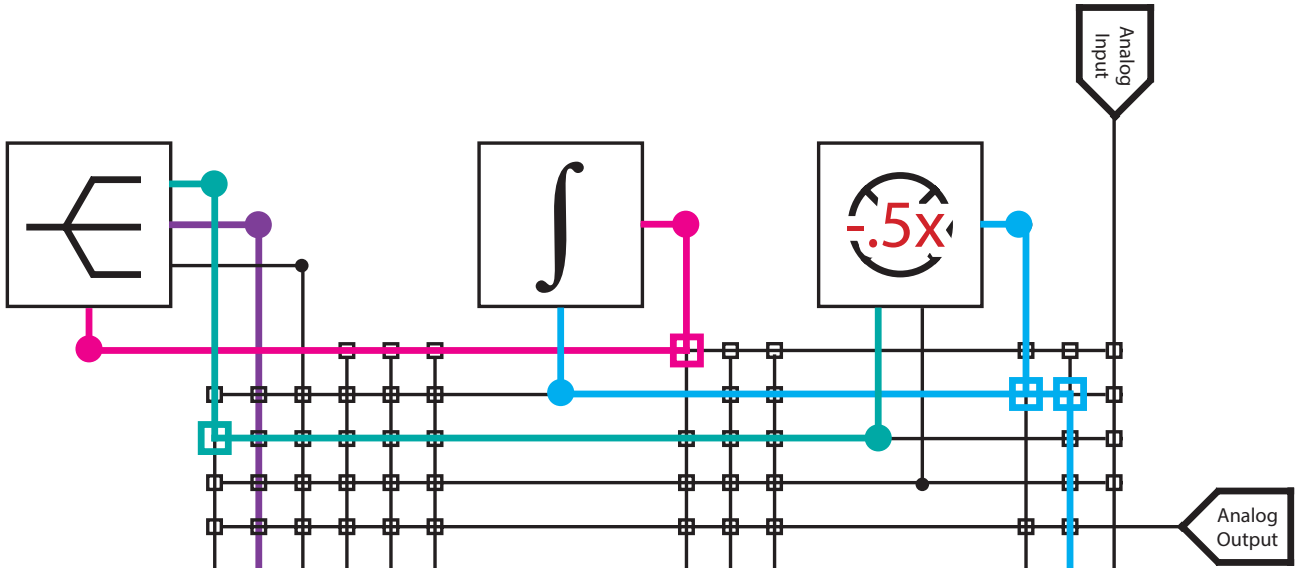
000000_000001_0010_10000000

Tile address, can address 64 tiles (chips)

Functional unit address, 000101 accesses the first integrator

Line address, 0010 sets the initial condition of the integrator

Value, 1000000_2 is middle value of the range we chose for the initial condition



Example: Configuration Message

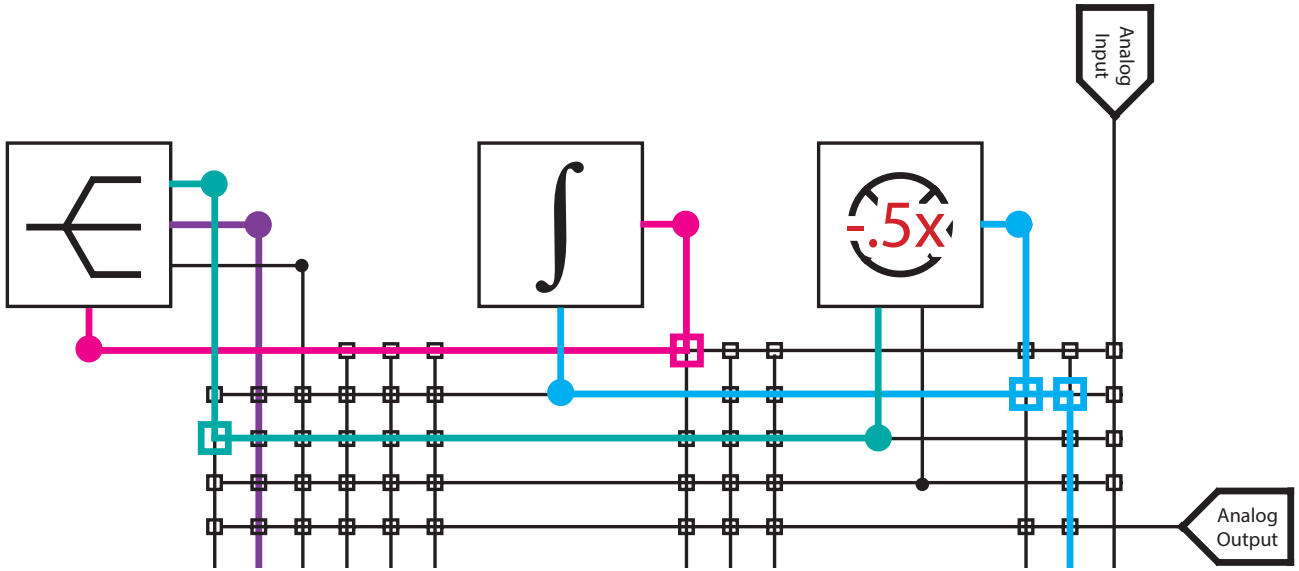
000000_000001_0101_10000000

Tile address, can address 64 tiles (chips)

Functional unit address, 000101 accesses the first integrator

Line address, 0101 sets the output destination of the integrator

Value, setting the first bit sends the output to the fanout unit



Example: Configuration Message

000000_000001_0101_00110000

Tile address, can address 64 tiles (chips)

Functional unit address, 0000001 accesses the tile controller

Line address, 0101 accesses the lowest timeout setting register

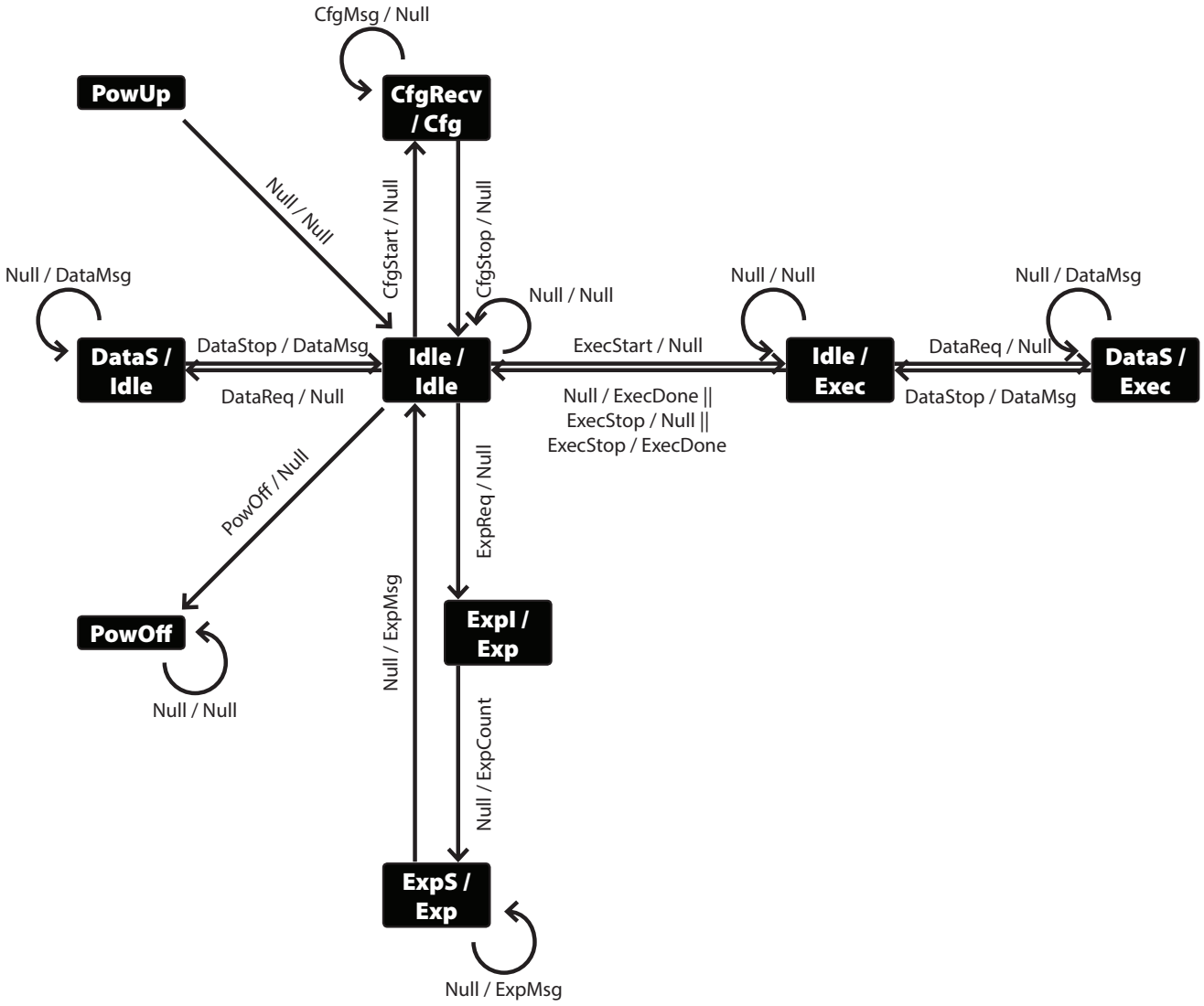
Value, 00110000_2 is 48_{10}, so simulator will run for 48 clock cycles, or 68.6 µs

Chip Configuration Protocol

- Tables describe addresses to access:
  - Datapath switches
  - Parameters
  - Lookup table entries
  - Simulation timer

		bits [9:11]							
		000	001	010	011	100	101	110	111
bits [6:8]	000	Unmapped	Tile controller addresses and data [xx,xx, 00,000,001] (See Tile Controller Bits 12:23])	Unmapped	(0,0) FAN configuration and crossbar messages (See FAN and CB Bits [12:23])	(0,1) FAN configuration and crossbar messages (See FAN and CB Bits [12:23])	(0,2) INT configuration and crossbar messages (See INT and CB Bits [12:23])	(0,3) MUL configuration and crossbar messages (See MUL and CB Bits [12:23])	(0,4) MUL configuration and crossbar messages (See MUL and CB Bits [12:23])
	001	(5,1) LUT configuration and crossbar messages (See LUT Bits [12:23])	(5,2) LUT configuration and crossbar messages (See LUT Bits [12:23])	Unmapped	(1,0) FAN configuration and crossbar messages (See FAN and CB Bits [12:23])	(1,1) FAN configuration and crossbar messages (See FAN and CB Bits [12:23])	(1,2) INT configuration and crossbar messages (See INT and CB Bits [12:23])	(1,3) MUL configuration and crossbar messages (See MUL and CB Bits [12:23])	(1,4) MUL configuration and crossbar messages (See MUL and CB Bits [12:23])
	010	(4,1) ADC configuration and crossbar messages (See ADC Bits [12:23])	(4,2) ADC configuration and crossbar messages (See ADC Bits [12:23])	Unmapped	(2,0) FAN configuration and crossbar messages (See FAN and CB Bits [12:23])	(2,1) FAN configuration and crossbar messages (See FAN and CB Bits [12:23])	(2,2) INT configuration and crossbar messages (See INT and CB Bits [12:23])	(2,3) MUL configuration and crossbar messages (See FU and CB Bits [12:23])	(2,4) MUL configuration and crossbar messages (See FU and CB Bits [12:23])
	011	(4,3) DAC configuration and crossbar messages (See DAC Bits [12:23])	(4,4) DAC configuration and crossbar messages (See DAC Bits [12:23])	Unmapped	(3,0) FAN configuration and crossbar messages (See FAN and CB Bits [12:23])	(3,1) FAN configuration and crossbar messages (See FAN and CB Bits [12:23])	(3,2) INT configuration and crossbar messages (See INT and CB Bits [12:23])	(3,3) MUL configuration and crossbar messages (See FU and CB Bits [12:23])	(3,4) MUL configuration and crossbar messages (See FU and CB Bits [12:23])
	100	LUT 1 addresses and data (prefix = [xx,xx,00,10x,xxx]) (See SRAM and LUT Bits [8:23])							
	101								
	110	LUT 2 addresses and data (prefix = [xx,xx,00,11x,xxx]) (See SRAM and LUT Bits [8:23])							
	111								

Simulation Control Over SPI



System State
Power up
Calibration
Configuration request
Configuration send
Timeout setting
Execution Start
Execution Stop
Exception request
Exception receive
Digital data output request
Digital data output receive
Power down

Chip Operation Timing

	Value
SPI interface clock frequency	16.7 MHz
Tile controller clock frequency	700 KHz
Time to complete configuration	2.08 ms
Time to complete calibration	1.10 ms
Maximum execution time	1.70 hours

Future Work

- HCDC system test bench
- HCDC compiler
- HCDC software library
- HCDC programming language

HCDC Robotics Workloads

Robots Profiled on Simulators

- Cornell Ranger Simulator
- ROS Gazebo Simulator
  - Turtlebot
  - PR2 mobile base

Candidate Code for HCDC Acceleration

- Sensory input processing
  - Odometry
  - Accelerometer and gyroscope input interpretation
  - Laser rangefinder input interpretation
- Kinematics
  - 3D transforms: translation, rotation
- Mapping
  - Point cloud best fit

- CAVEAT: digital overheads dominate robot runtime
  - ROS kernel
  - Communication routines