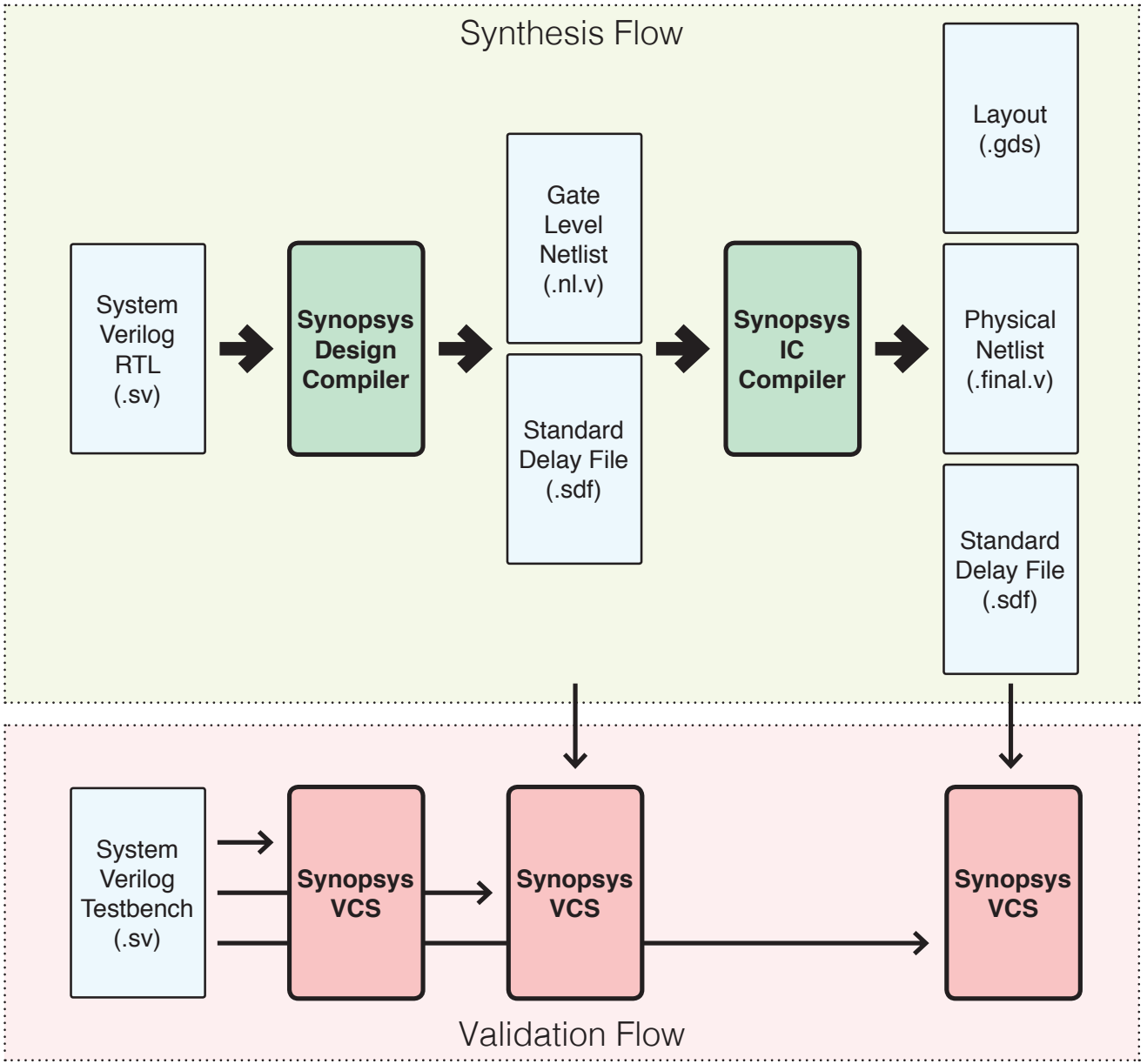
Logic and physical synthesis



What is digital logic synthesis?

- Turn your SystemVerilog RTL design into a schematic (.nl.v file) + timing information (.sdf file)

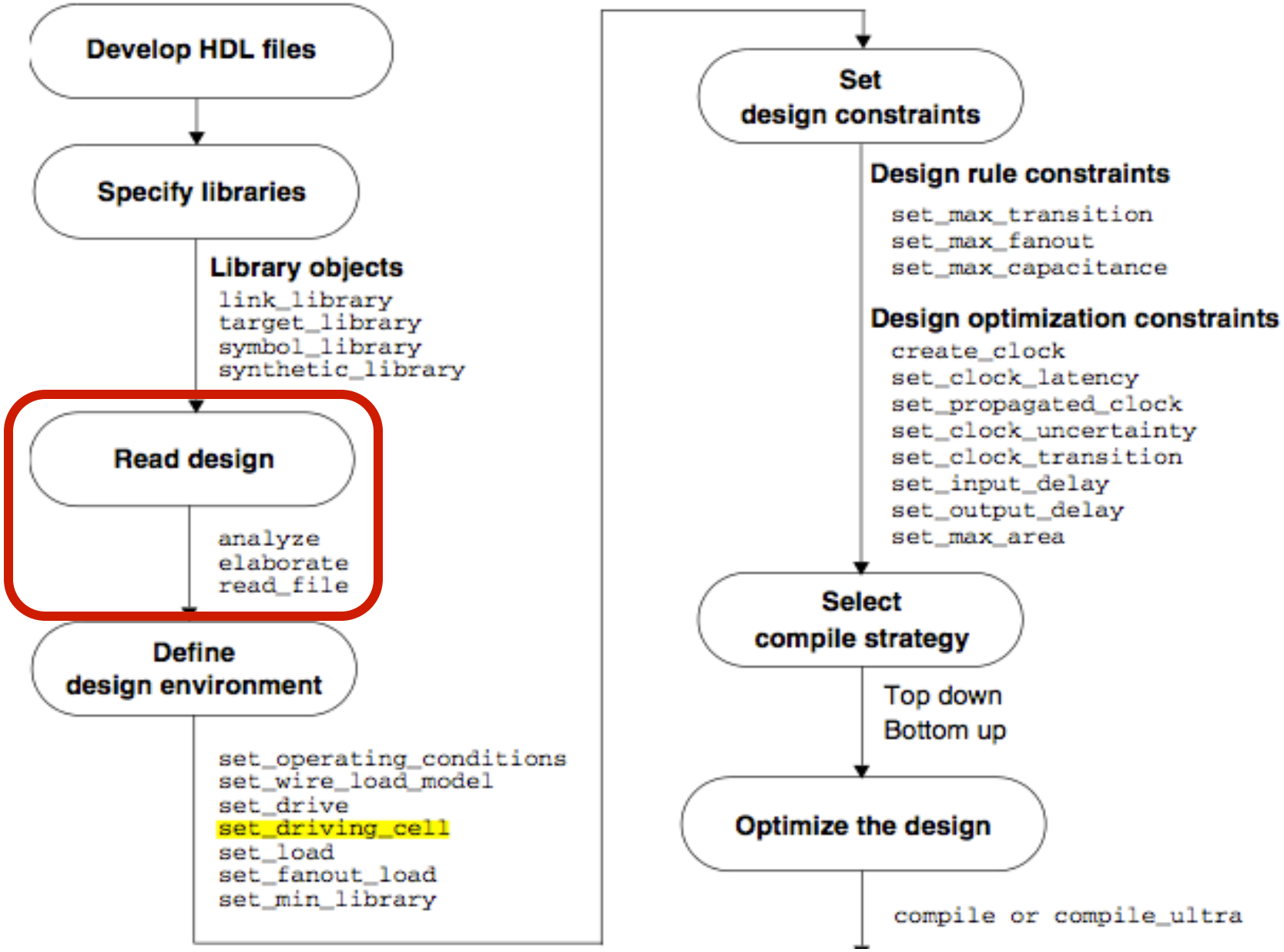
- What is a logic netlist?
  - A design consisting of standard cells that has same functional behavior

- Let’s look at an example digital logic netlist

Netlist compilation demo

- Download & unpack digital_synthesis.tar.gz
- source /sim/synopsys64/env_castl.sh
- make dc
- make dc_view
- The following slides explain the steps in dsyn.tcl

Digital synthesis roadmap

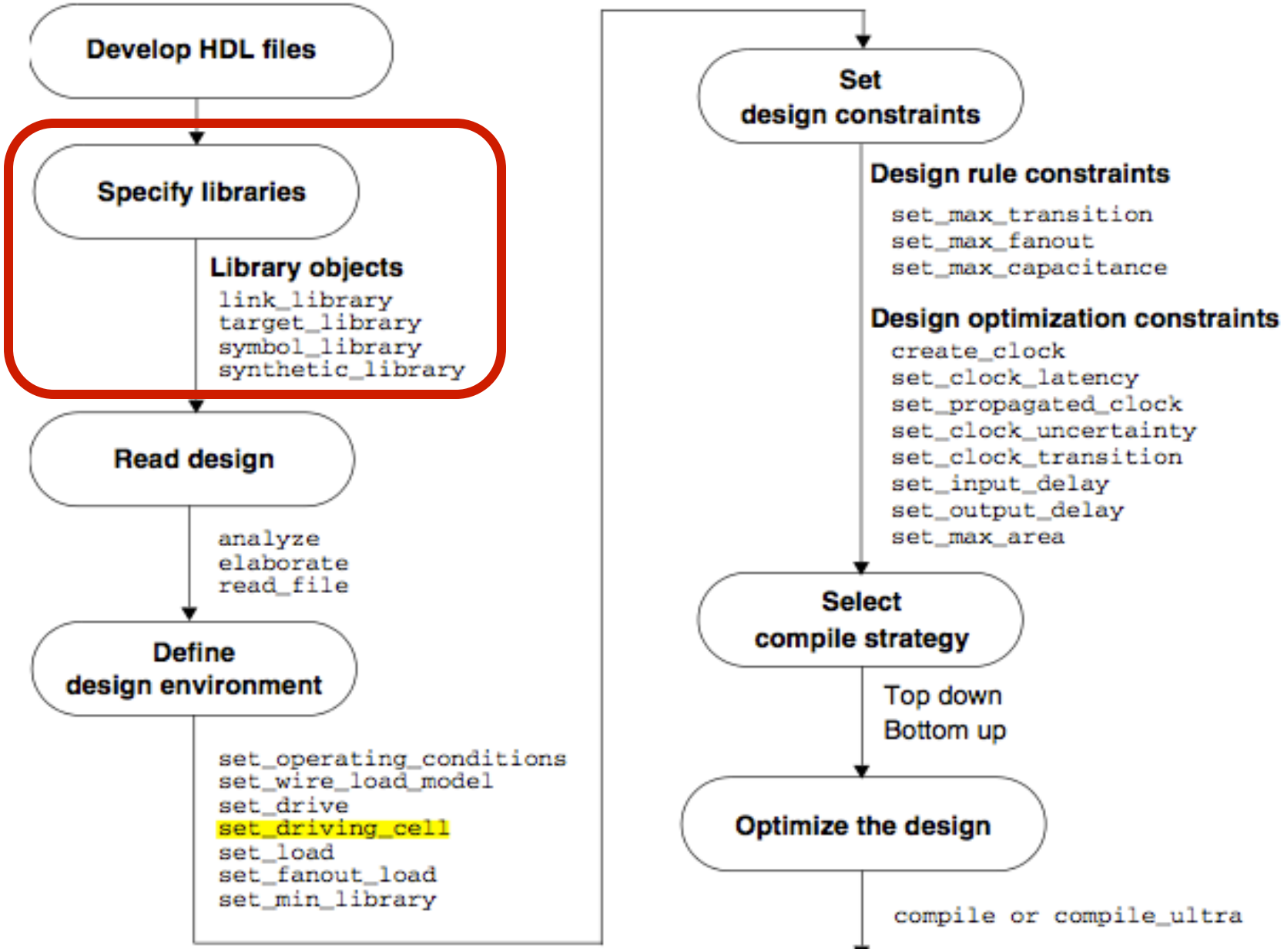


Source: Design Compiler User Guide

Read design

- Edit the file dsyn.tcl; you must change the lines:
  - set myFiles [glob ../../*.sv]; # RTL source files
  - set basename cam; # Top-level module name
  - set CLK "clk"; # The name of your clock

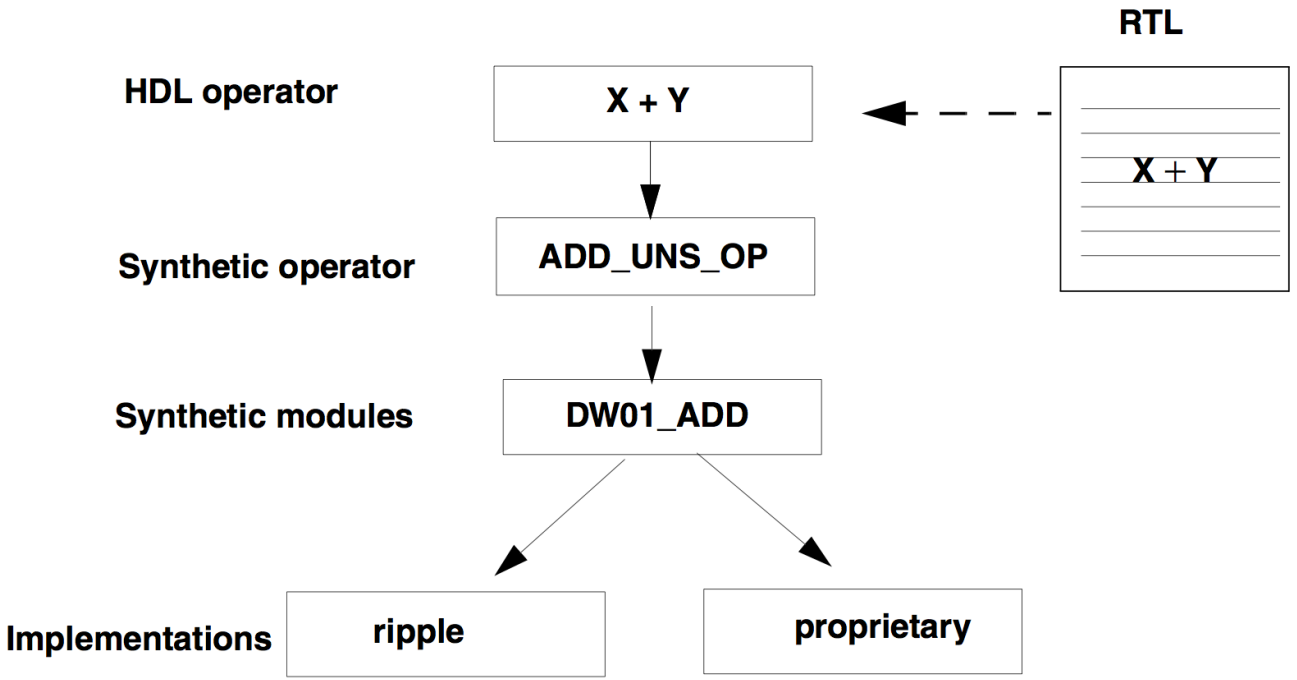
Digital synthesis roadmap



Synthesis libraries: IP designs

- Libraries provides IP to logic synthesis to build your design
  - How does a simple '+' operator in SystemVerilog become hardware?

- Synthetic library:



- Full list of Synopsys DesignWare IP components at
  - /sim/synopsys64/icc/dw/doc/manuals/dwbb_quickref.pdf

Synthesis libraries: standard cells

- Logic synthesizer then builds seq. and comb. logic as gates

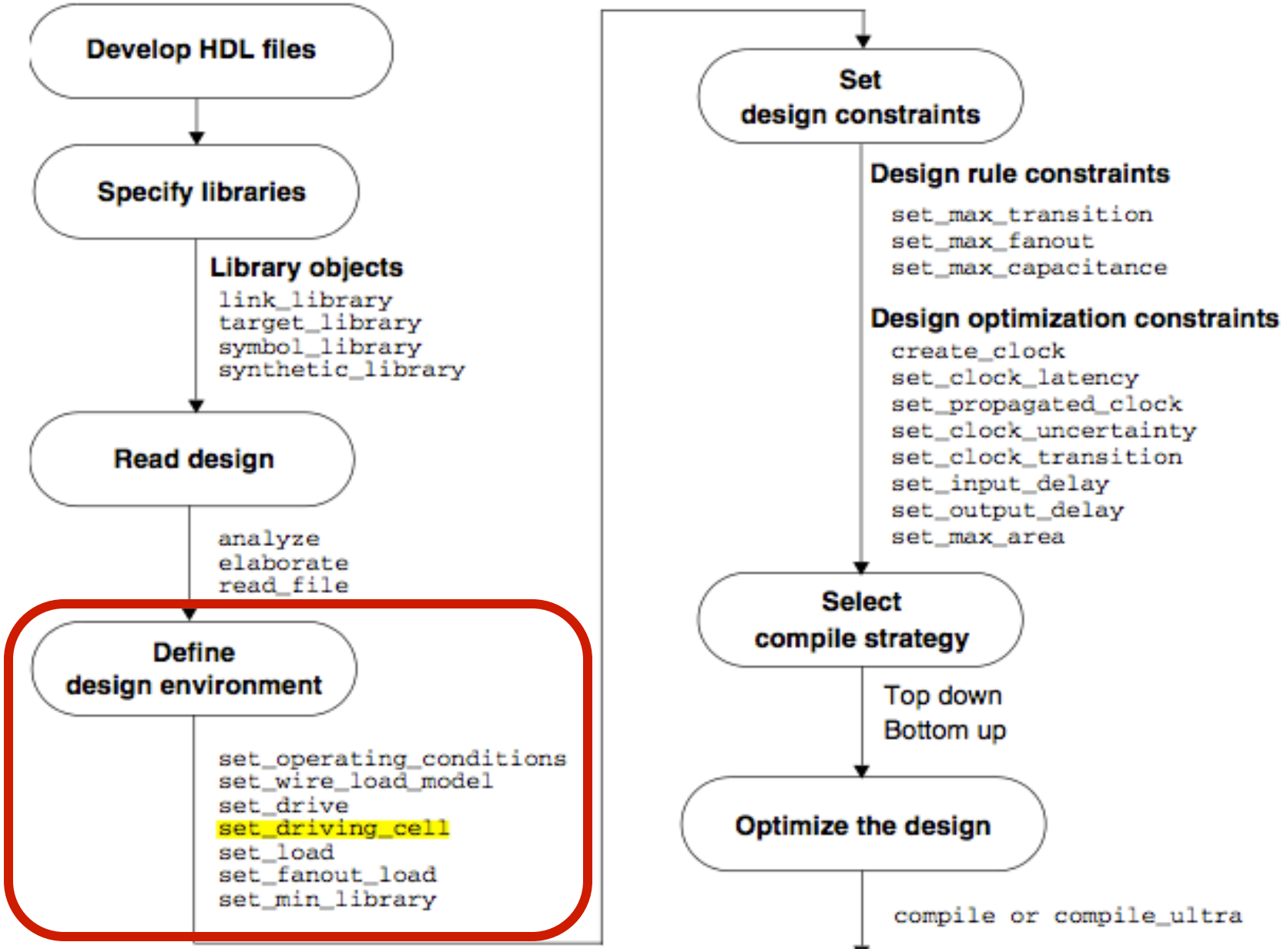
Table 9.10. AND Electrical Parameters and Areas

Cell Name	Operating Conditions: VDD=1.2 V DC, Temp=25 Deg.C, Operating Frequency: Freq=300 MHz, Capacitive Standard Load: Csl=13 fF				Area
	Cload	Prop Delay (Avg)	Power		
			Leakage (VDD=1.32 V DC, Temp=25 Dec.C)	Dynamic	
		ps	nW	nW/MHz	(um^2)
AND2X1	1 x Csl	85	298	19	7.3728
AND2X2	2 x Csl	96	568	36	8.2944
AND3X1	1 x Csl	119	297	34	8.2944
AND3X2	2 x Csl	135	562	55	10.1376
AND4X1	1 x Csl	129	299	42	10.1376
AND4X2	2 x Csl	147	574	75	11.9808

- Full list of 90nm digital standard cells at:
  - /sim/synopsys/SAED_EDK90nm/Digital_Standard_Cell_Library/doc/cell_list/saed90nm.cellList

- Standard cell databook
  - /sim/synopsys/SAED_EDK90nm/Digital_Standard_Cell_Library/doc/databook/SAED_Digital_Standard_Cell_Library_Rev1_8_2009_11_30.pdf

Digital synthesis roadmap



Source: Design Compiler User Guide

The job of the design compiler

- There are many IP designs and gates to choose from
  - Which ones to select?
- Logic synthesizer balances optimization targets…
  - Timing, area, power
- Subject to varying operating conditions…
  - Temperature, supply voltage, semiconductor doping variability
- Subject to constraints imposed by design's inputs & outputs…
  - Drive strength & timing delay given at the inputs
  - Fanout load & timing slack demanded at the output
- To create functionally equivalent digital logic netlist

Operating condition & wire model

- set_operating_conditions: refer to standard cell databook

Parameter	Min	Typ	Max	Units
Power Supply (VDD) range	0.7	1.2	1.32	V
Operating Temperature range	-40	+25	+125	°C
Operating Frequency (F)	-	300	-	MHz

- set_wire_load_model: refer to report/report_lib.rpt

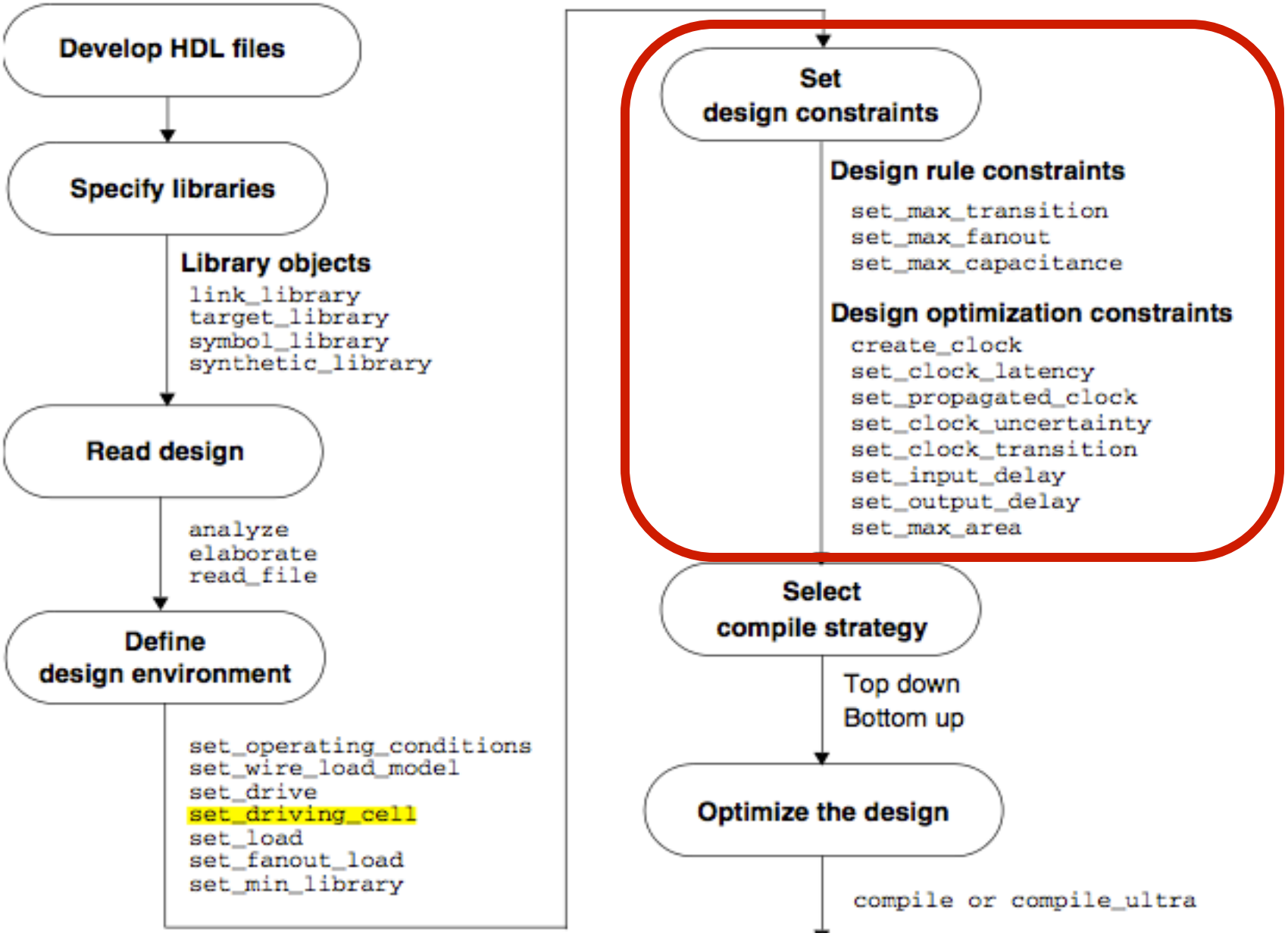
```
 Selection             Wire load name
     min area    max area
    ----------------------------------------
…
       200.00     8000.00           8000
      8000.00    16000.00           16000
…
Fanout   Length   Points Average Cap Std Deviation
------------------------------------------------------------
      1    13.94
      2    31.80
…
```

Input drive strength & output load

- set_driving_cell
  - Standard capacitance (C_{sl}) is input capacitance of the fanout-of-four inverter
- set_fanout_load

Drive Strength	Cell Load
X0	0.5x C_{sl}
X1	1x C_{sl}
X2	2x C_{sl}
X3	3x C_{sl}
X4	4x C_{sl}
X8	8x C_{sl}
X12	12x C_{sl}
X16	16x C_{sl}
X24	24x C_{sl}
X32	32x C_{sl}

Digital synthesis roadmap



Source: Design Compiler User Guide

Clock: slew, jitter, skew, latency

- create_clk
- set_clk_uncertainty
  - Models slew, jitter, latency all in one command

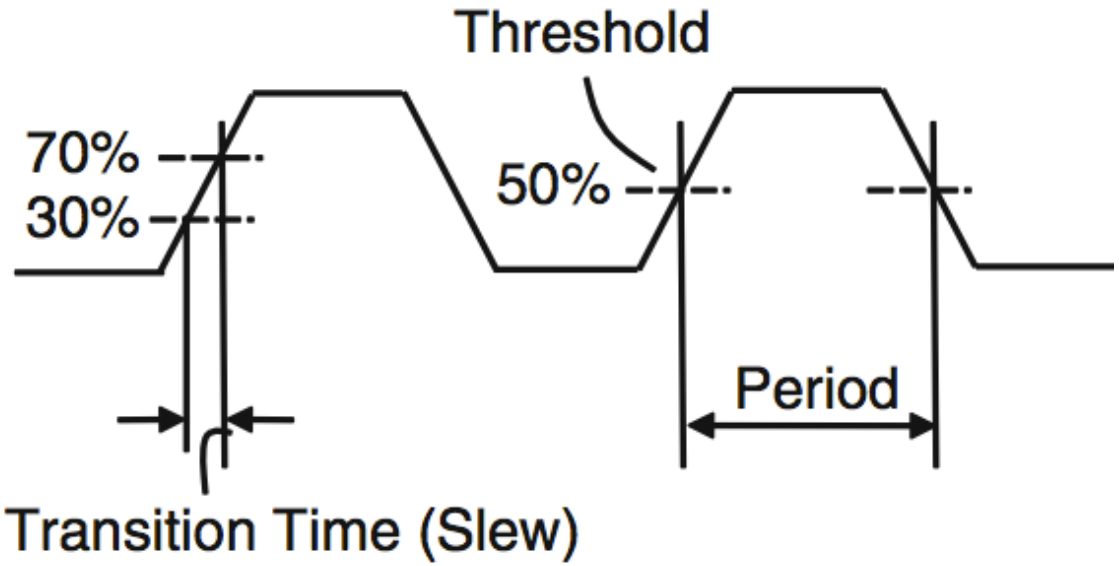
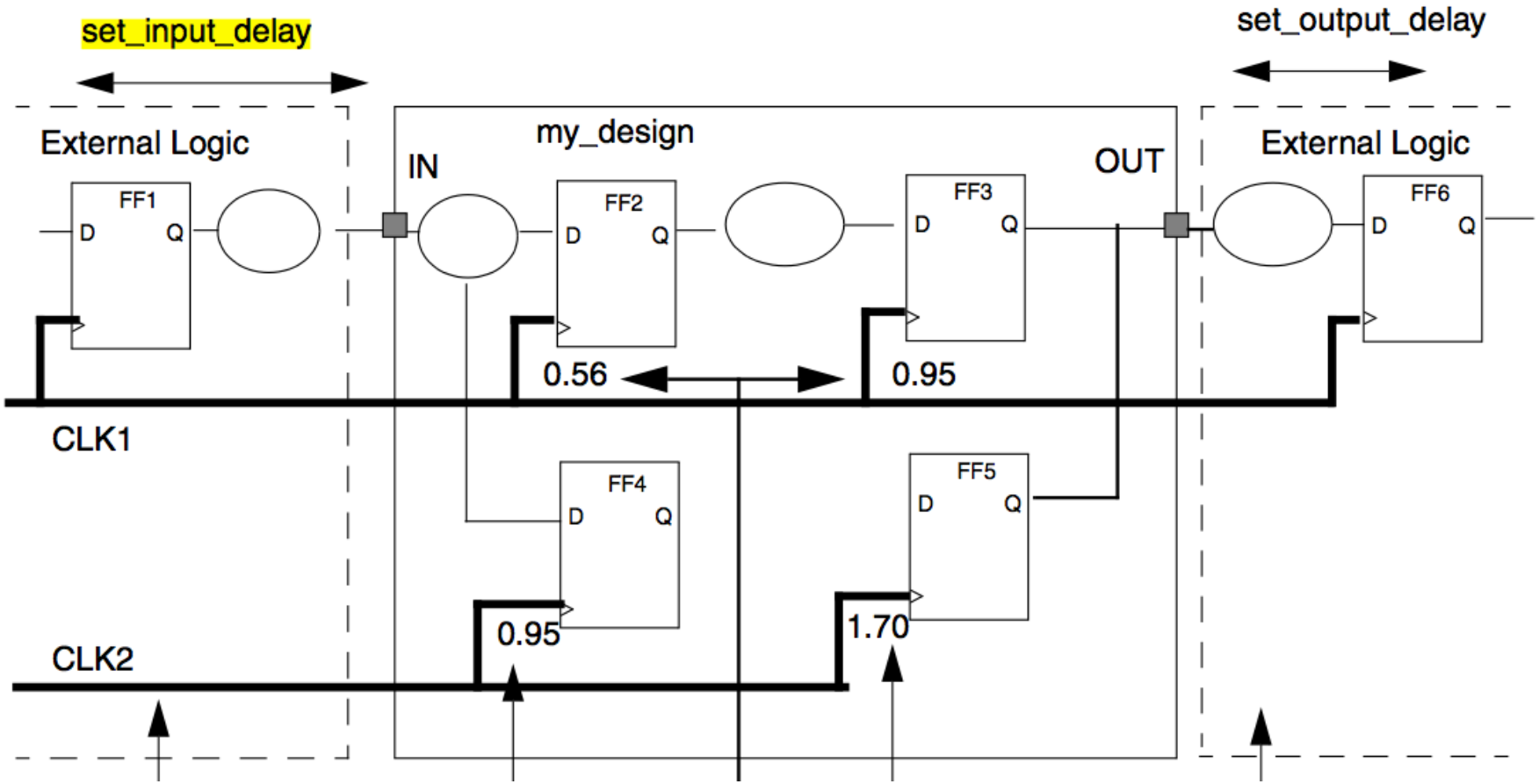


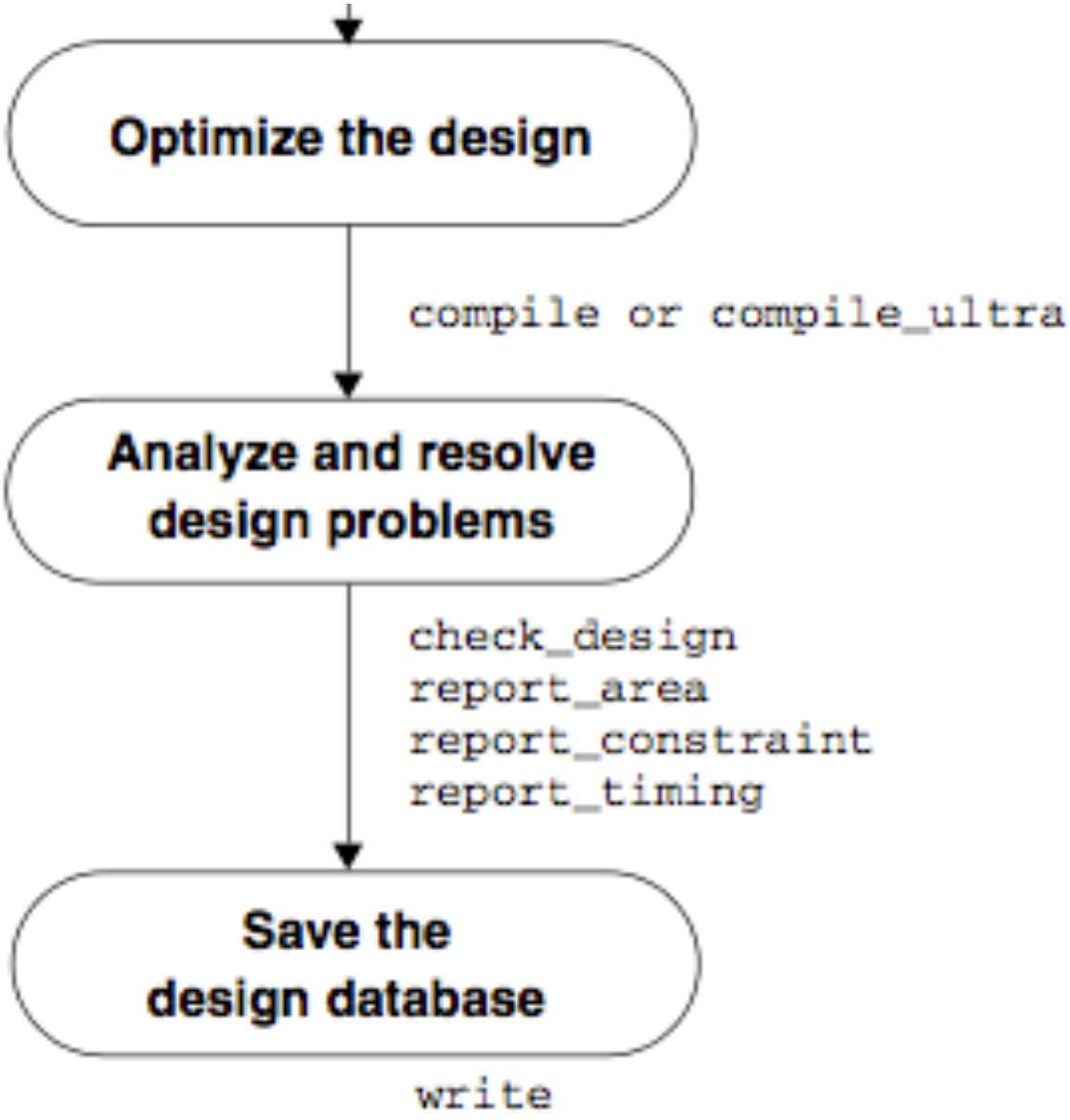
Fig. 8.1 Waveform of a non-ideal clock

Input & output delay

- set_input_delay
  - The modules giving us input have some combinational logic delay
- set_output_delay
  - The modules taking our output also demand some slack



Digital synthesis roadmap



References & citations

- Constraining Designs for Synthesis and Timing Analysis
  - A Practical Guide to Synopsys Design Constraints (SDC)
  - Available on Columbia network via SpringerLink
  - http://link.springer.com/book/10.1007%2F978-1-4614-3269-2

- DesignWare Datapath and Building Block IP Quick Reference
  - /sim/synopsys64/icc/dw/doc/manuals/dwbb_quickref.pdf

- Digital Standard Cell Library SAED_EDK90_CORE Databook
  - /sim/synopsys/SAED_EDK90nm/Digital_Standard_Cell_Library/doc/databook/SAED_Digital_Standard_Cell_Library_Rev1_8_2009_11_30.pdf

- Design Compiler User Guide
- Design Compiler Optimization Reference Manual
- Timing Constraints and Optimization User Guide