Continuous-Time Hybrid Computation with Programmable Nonlinearities

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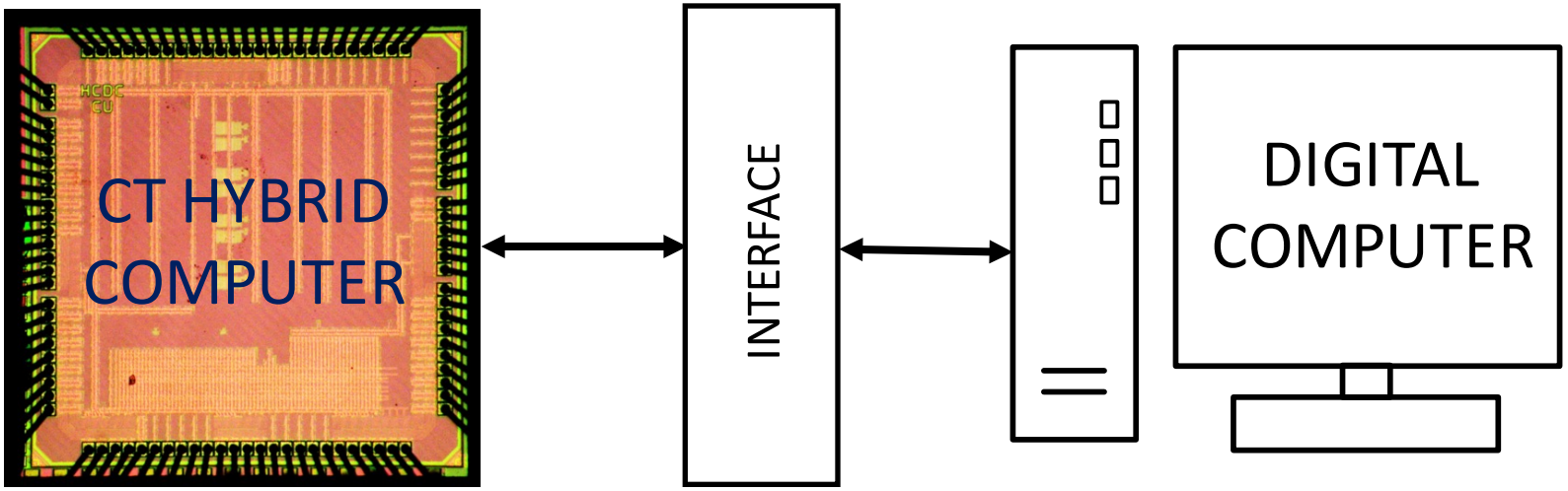
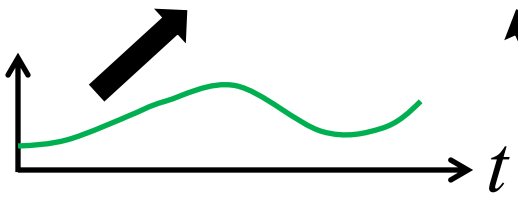
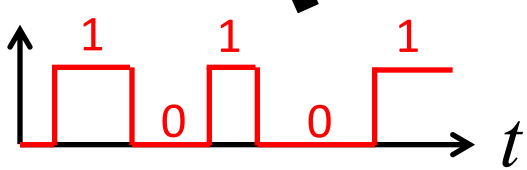
This talk presents a new principle:
Continuous-time hybrid computation







Synergy with a digital computer through a common interface

Both analog **and digital** signals are functions of continuous-time

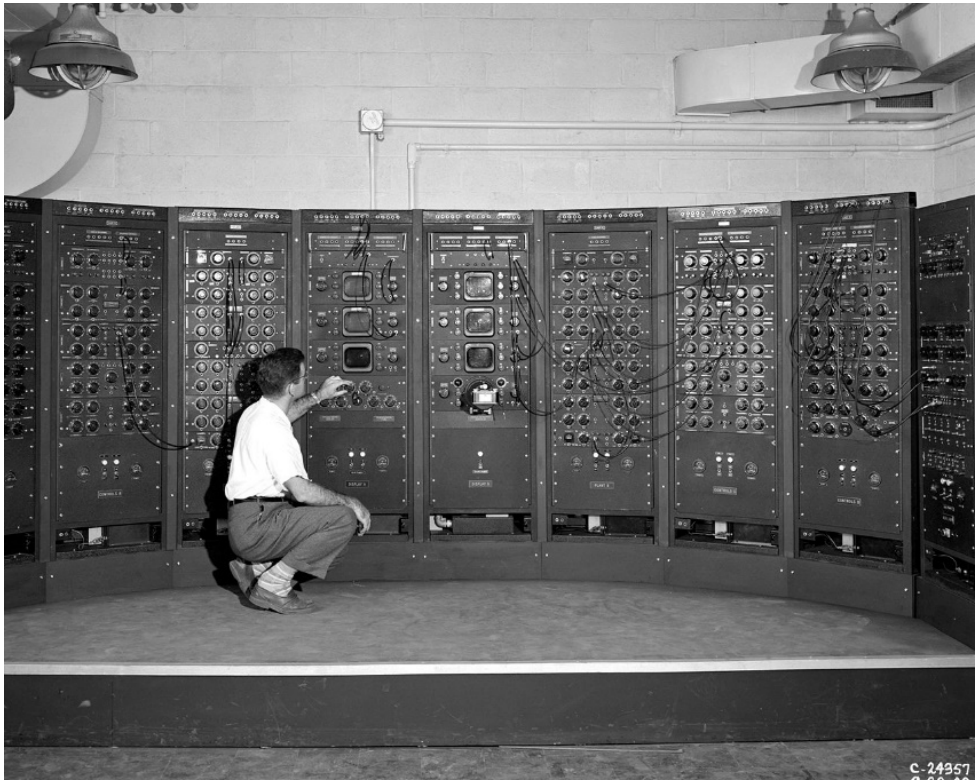
Time intervals: Important info, **unlike** the case in async digital.

Outline

1. Background and motivation
2. Math operations
3. System architecture
4. Circuit design
5. Measurement results
6. Conclusions

Background and motivation

- Analog computers were dominant in the 1960s; they helped send Man to the moon!
  - Solving ordinary/partial differential equations
  - Parallel computation
  - No convergence issues



https://en.wikipedia.org/wiki/Analog_computer

Background and motivation

- Analog computers were abandoned in the 1960s and 1970s, while they were still using the technology you saw on the previous slide.

- Their potential in modern VLSI technology was not considered until recently [1].

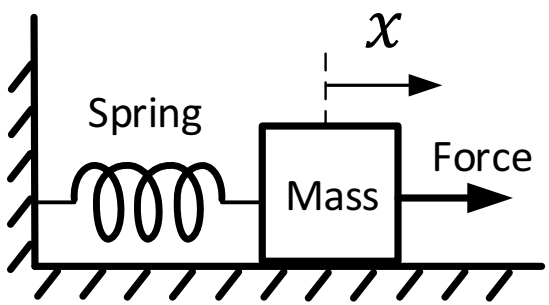
- It was shown that VLSI analog computers are suitable for:
  - Low-power, self-contained approximate computation
  - Speed-up of digital computation through co-processing.

[1] G. Cowan et al., ISSCC 2005

Background and motivation

Analog computation example

Physical system



Math equation:

$$\ddot{x} = -0.2\,\dot{x} - 0.5x + 1;$$

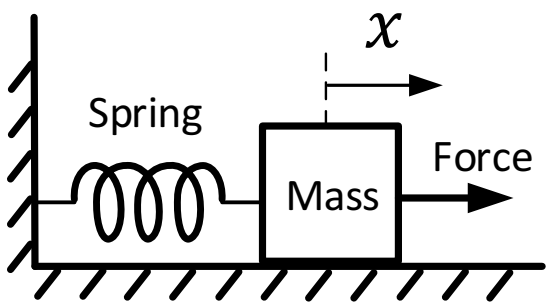
Initial conditions:

$$x(0) = 9;$$
$$\dot{x}(0) = -7$$

Background and motivation

Analog computation example

Physical system



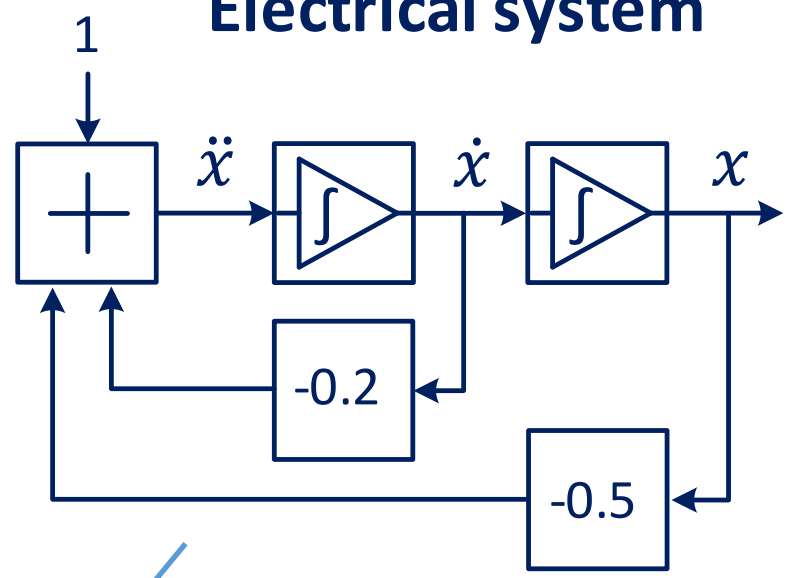
Math equation:

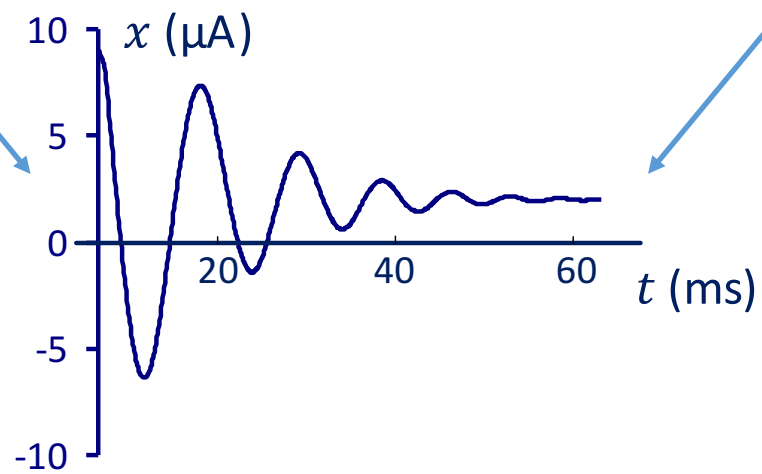
$$\ddot{x} = -0.2\,\dot{x} - 0.5x + 1;$$

Initial conditions:

$$x(0) = 9;$$
$$\dot{x}(0) = -7$$

Electrical system





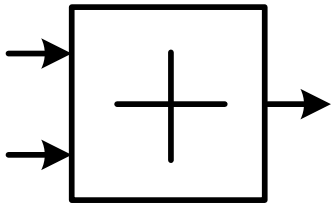
Background and motivation

- We present a new principle: *continuous-time hybrid computation*
  - Continuous-time analog computation
  - **Continuous-time digital** computation **NO CLOCK**

- Compared to the fully analog approach, the new approach results in:
  - Better accuracy
  - Higher programmability and generality

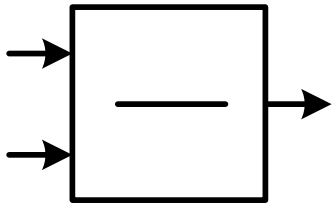
Math operations

Basic arithmetic operations:



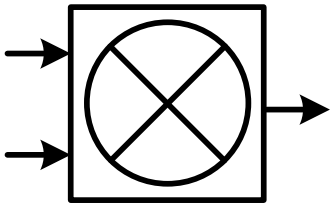
Addition

$$z(t) = x(t) + y(t)$$



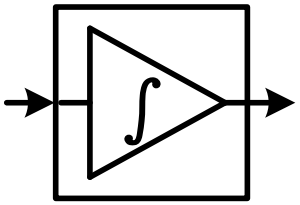
Subtraction

$$z(t) = x(t) - y(t)$$



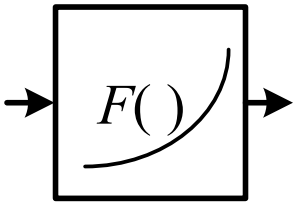
Multiplication

$$z(t) = x(t)y(t)$$



Integration

$$y(t) = \int_0^t x(\tau)\, d\tau$$



Nonlinear function

$$y(t) = F(x(t))$$

Math operations

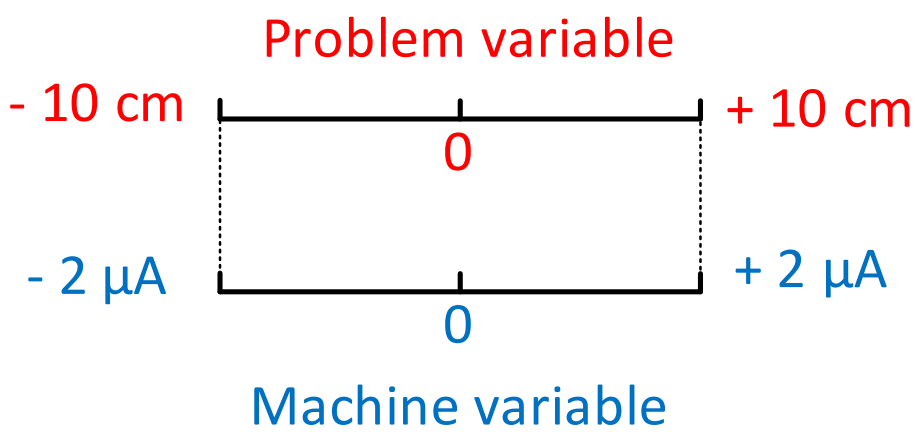
Amplitude scaling:

Problem variable

↓

Machine variable

Example:



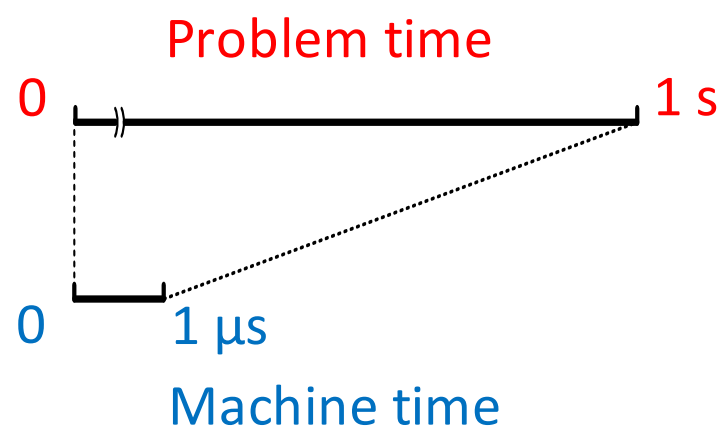
Time scaling:

Problem time

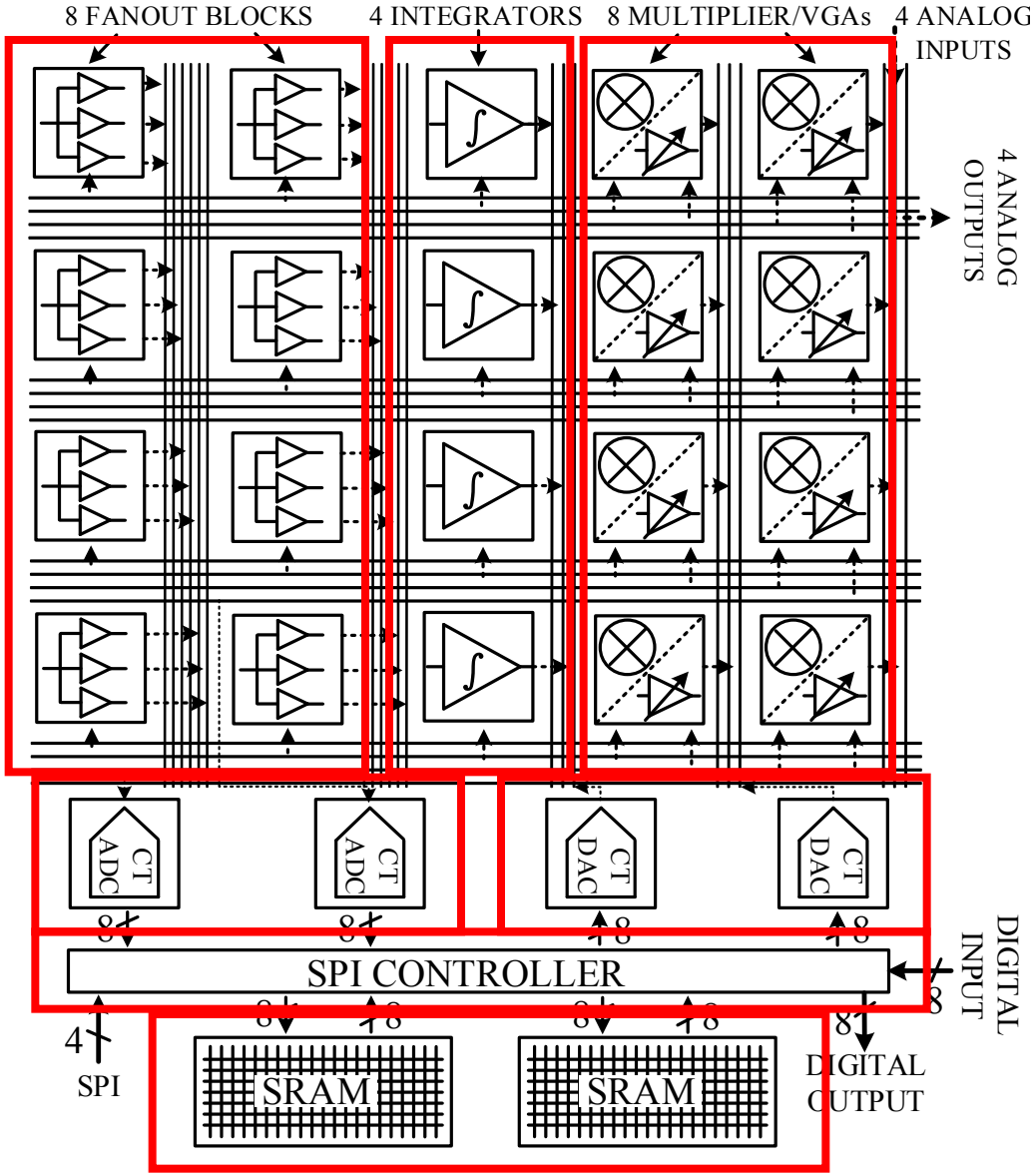
↓

Machine time

Example:



System architecture



Accuracy: 8-bit

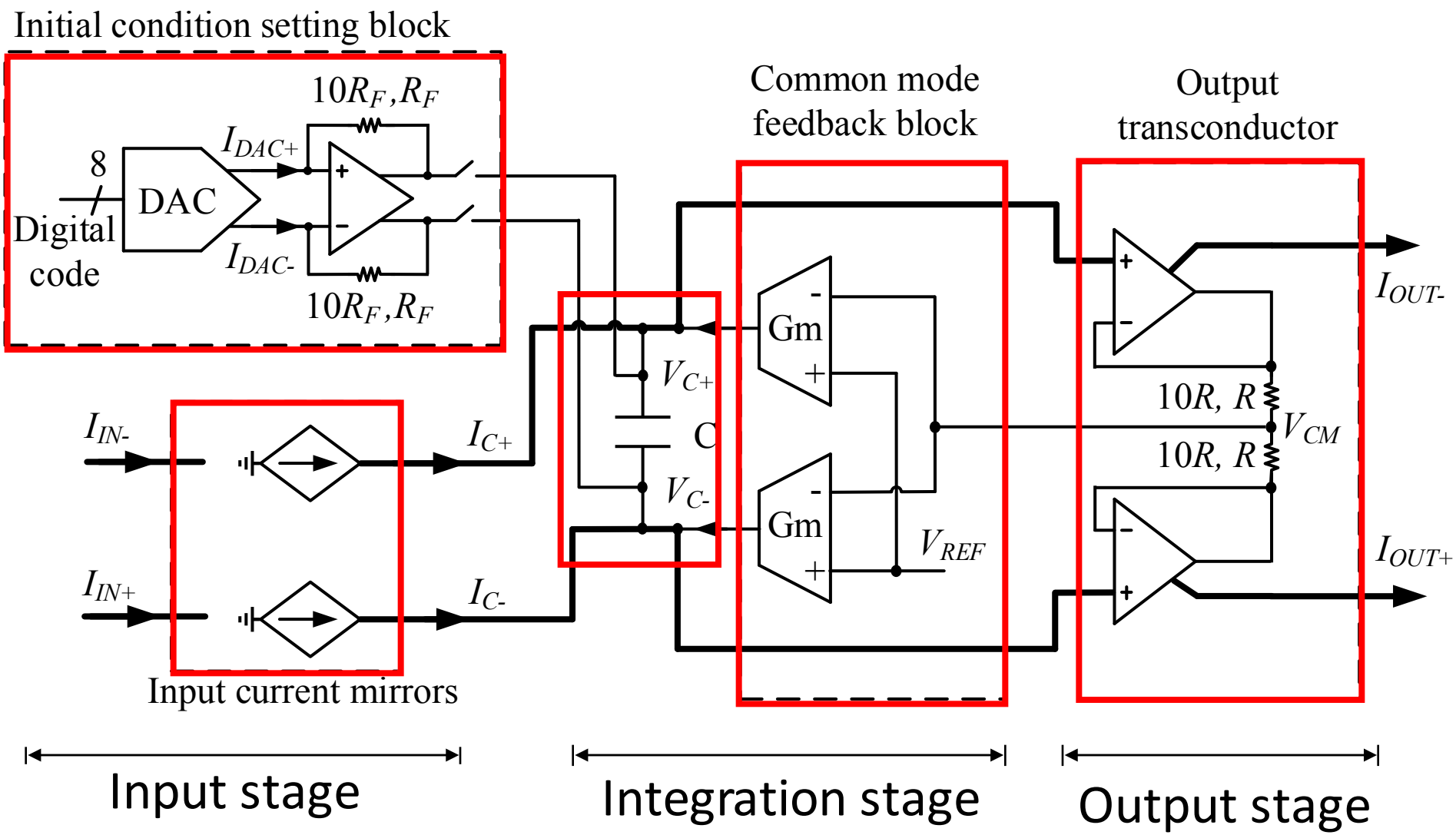
Signal representation:
Differential current

Analog block interface:
DC coupled, Class-AB

Offsets :
< 1 LSB after calibration

Analog signal bandwidth:
DC - 20 KHz

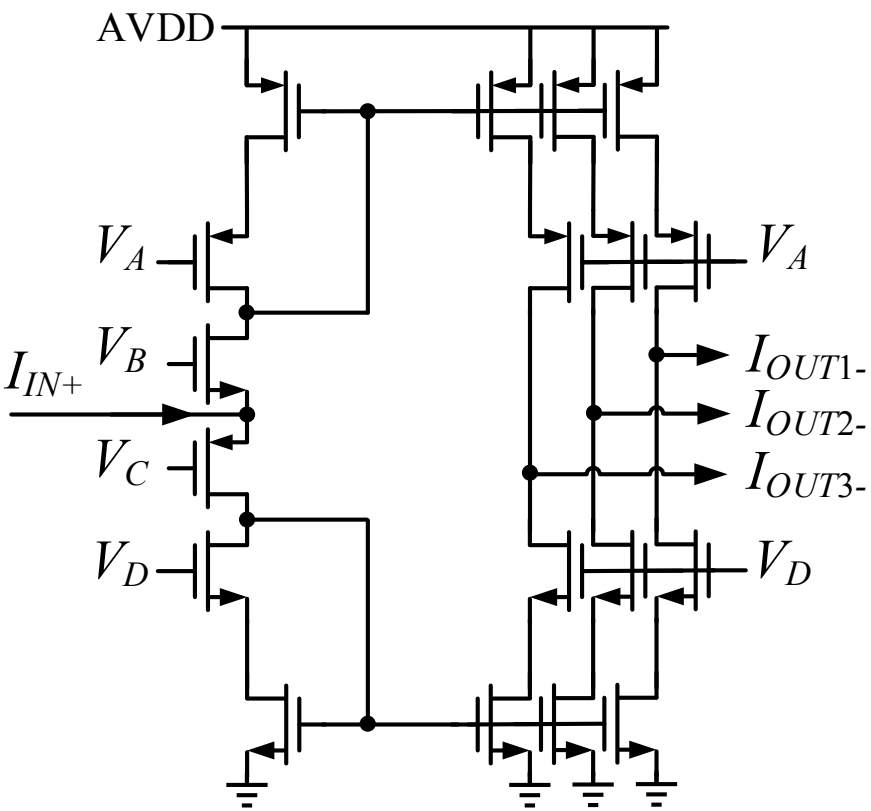
Circuit design: Integrator block



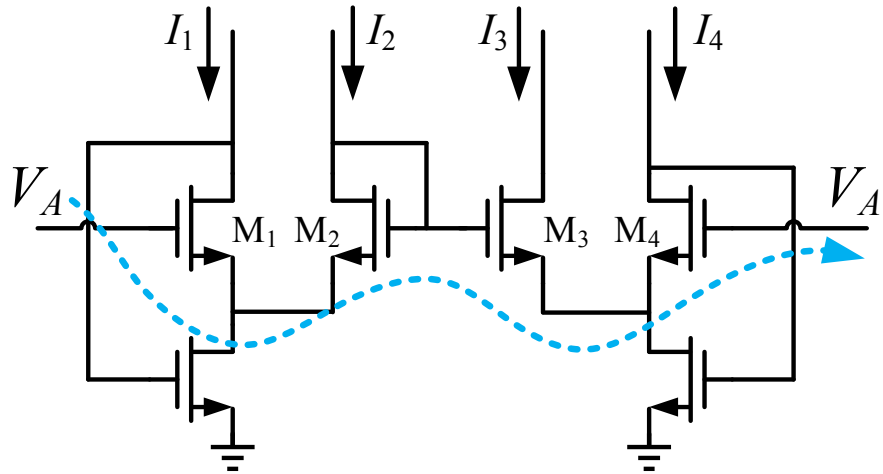
Circuit design

Circuit techniques used in other blocks:

Fanout block



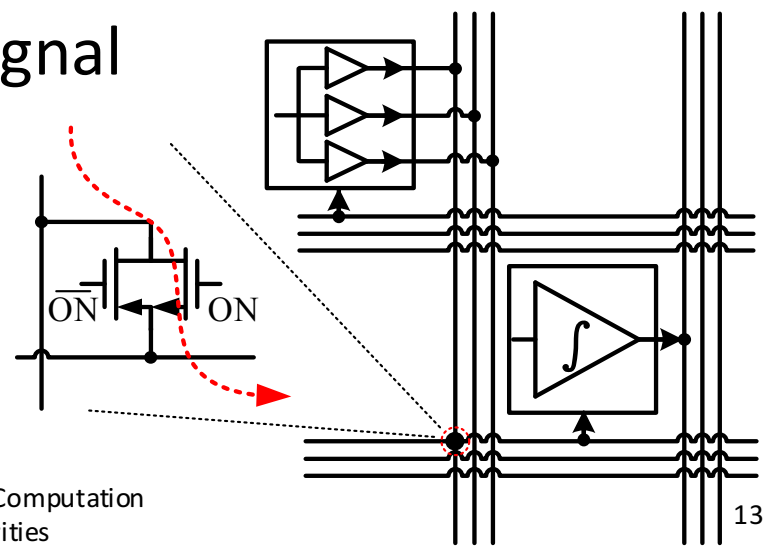
Multiplier block (principle)



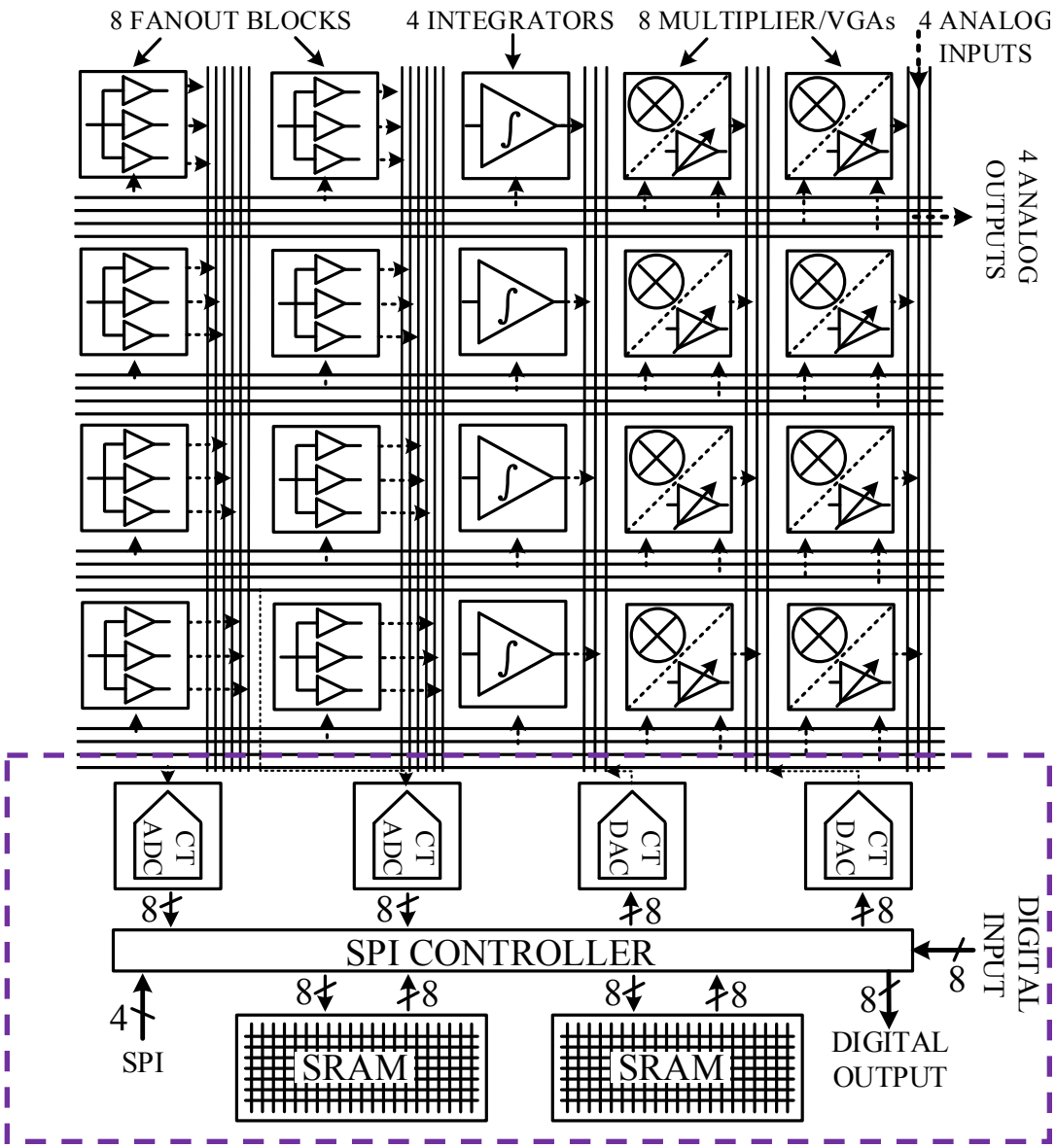
M_1, M_2, M_3, M_4 in weak inversion

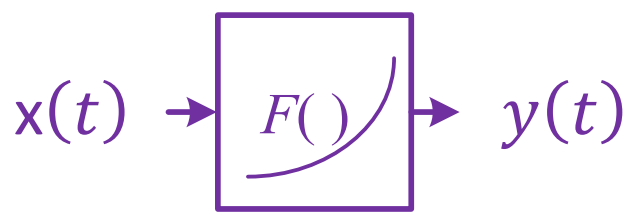
$$V_{GS1} + V_{GS3} = V_{GS2} + V_{GS4} \Rightarrow I_1 I_3 = I_2 I_4$$

Analog signal routing



System architecture



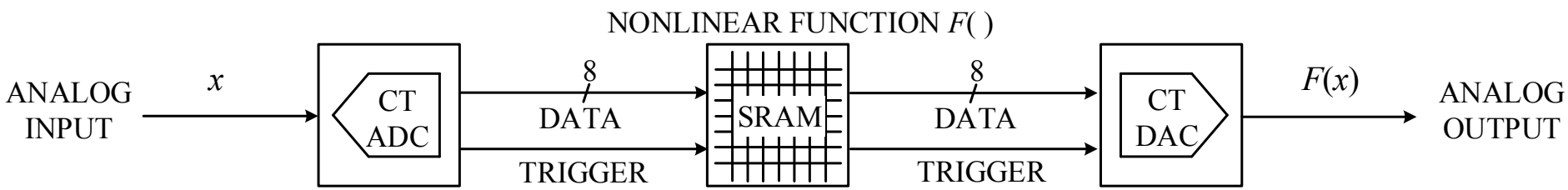


Nonlinear function

$$y(t) = F(x(t))$$

Circuit design: Nonlinear function block

Our approach: A **continuous-time** programmable lookup table



[2] B. Schell et al., ISSCC 2008

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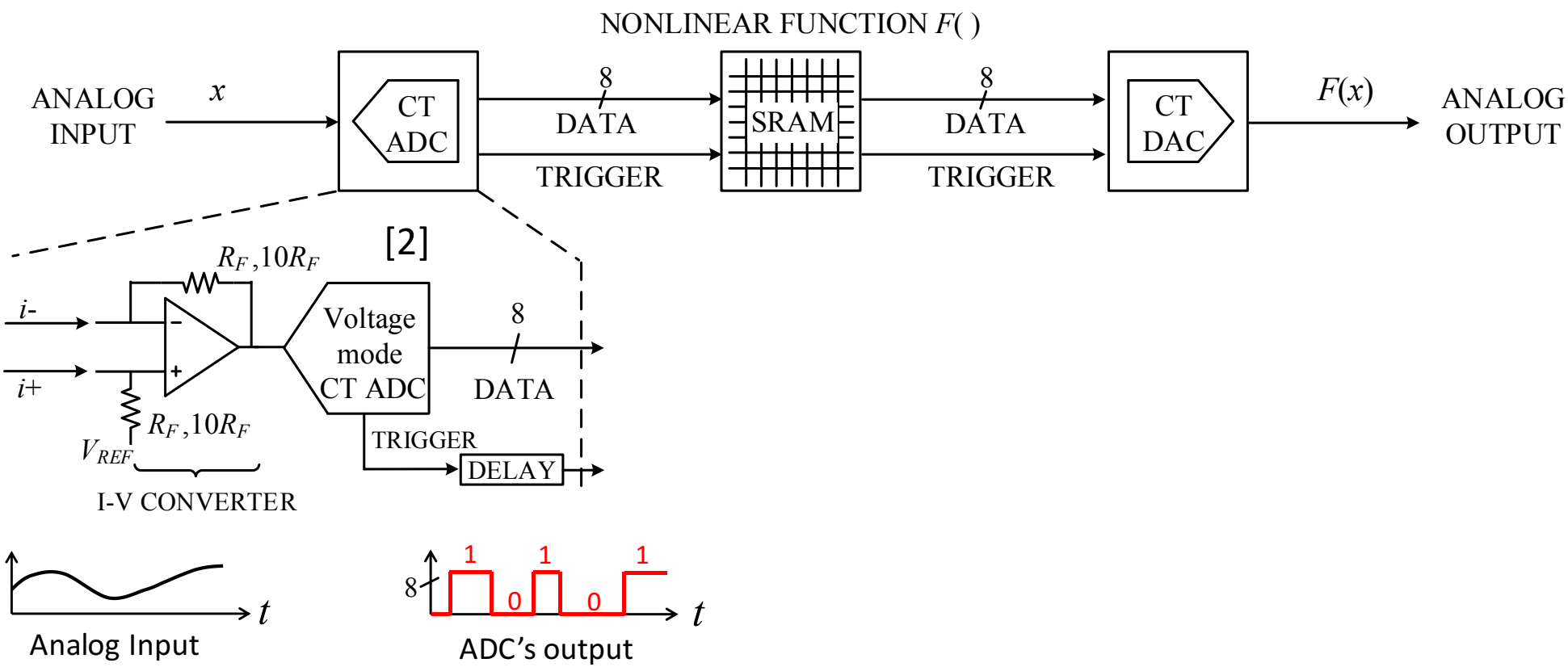
Advantages over discrete-time counterpart:

- **Activity-dependent** power dissipation
- **Faster response** to input changes
- **No aliasing**

Circuit design: Nonlinear function block

Implementation:



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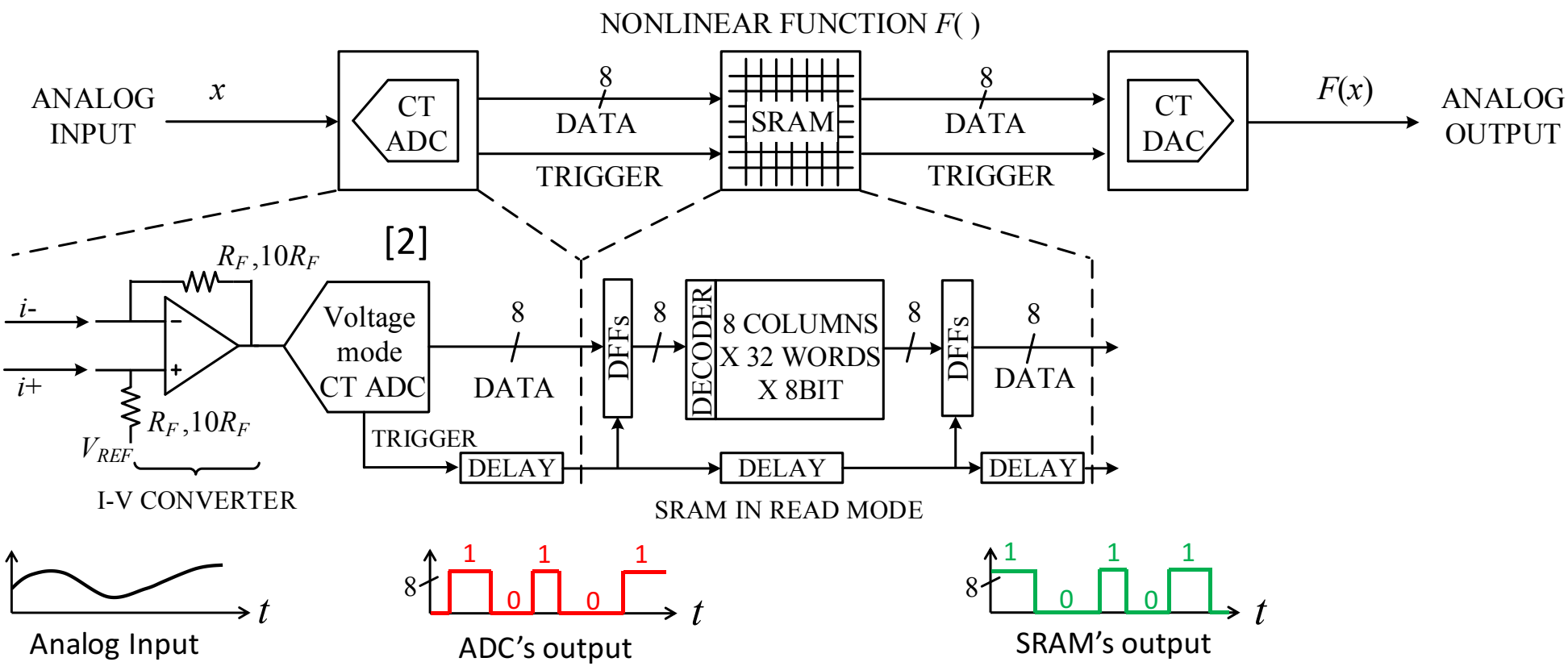
[2] B. Schell et al., ISSCC 2008

Circuit design: Nonlinear function block

Implementation:



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Circuit design: Nonlinear function block

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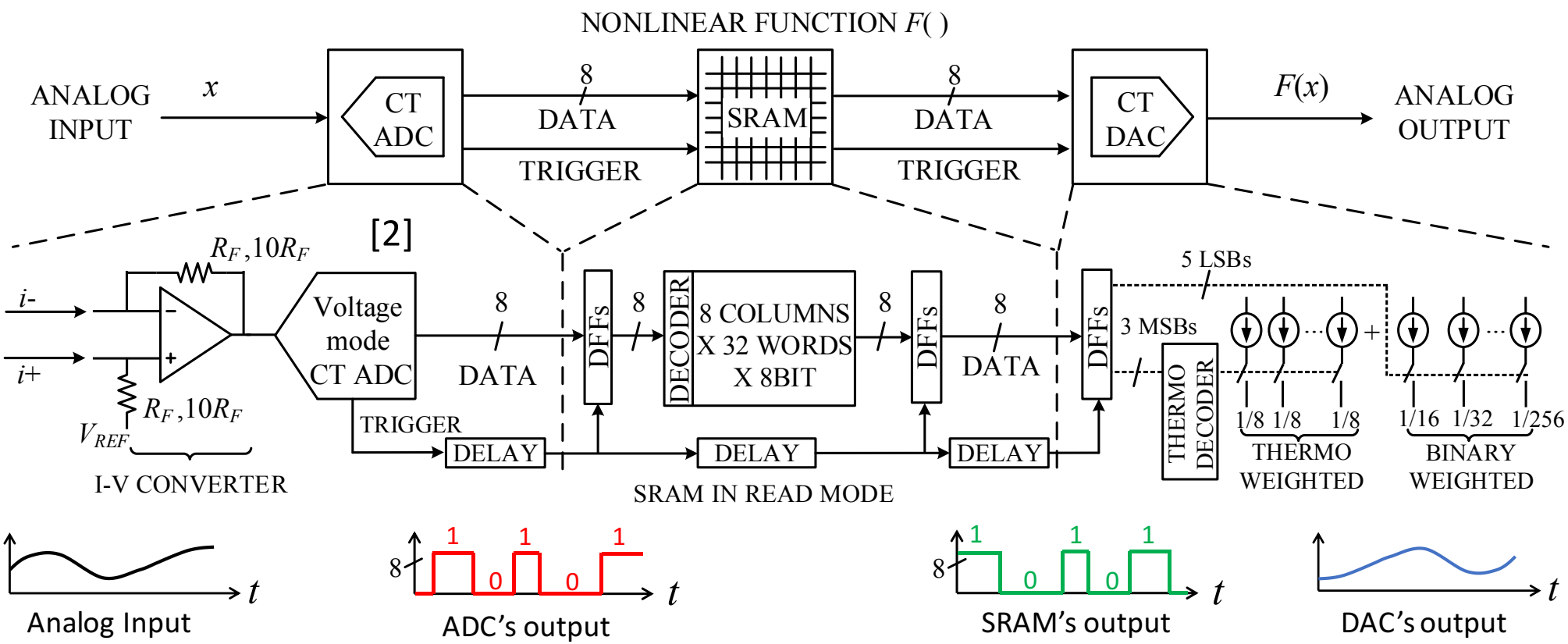

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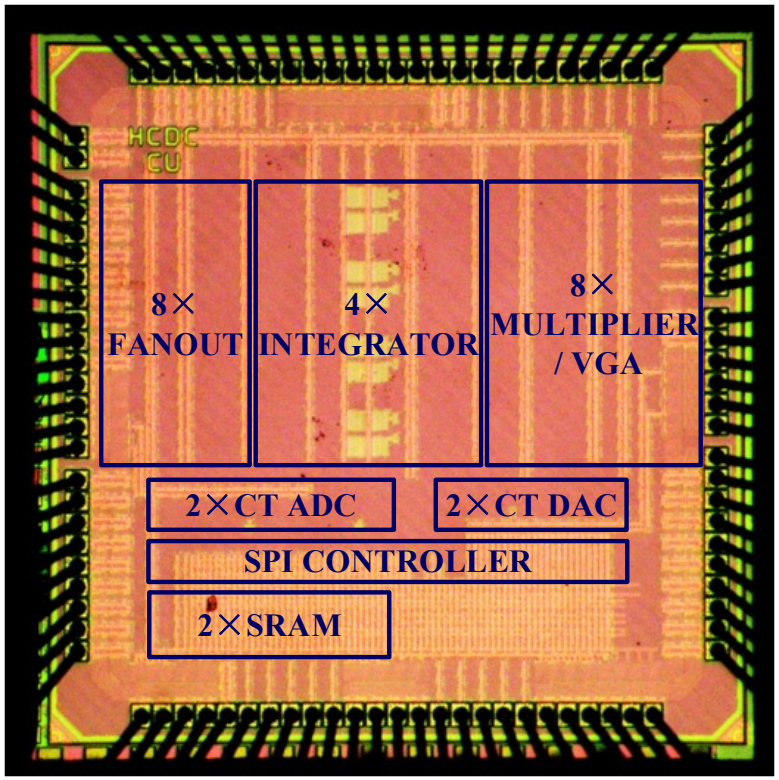
Measurement results

Die photo



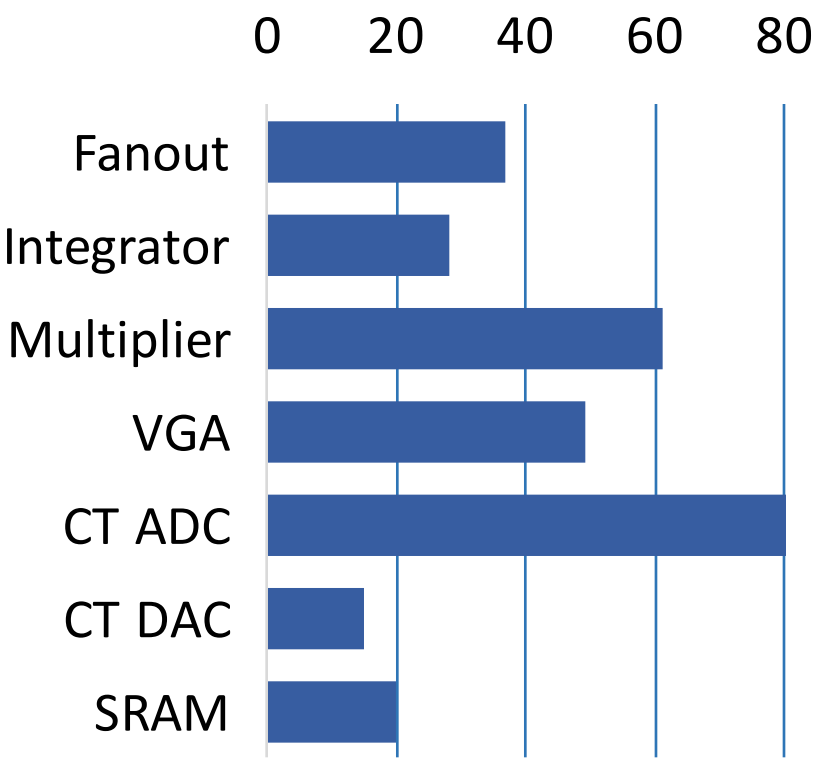
Key performance summary*

Supply voltage	1.2V
Technology	TSMC 65nm LP
Die area/active area	3.8 mm² / 2.0 mm²
Integrator nonlinearity	0.44%
Fanout nonlinearity	0.13%
Multiplier/VGA nonlinearity	0.15%
ADC+DAC SNDR @20KHz	53dB
DAC DNL / INL	0.73 LSB / 0.67 LSB

*Measurement conditions listed in Digest paper

Measurement results

Power dissipation* (µW)



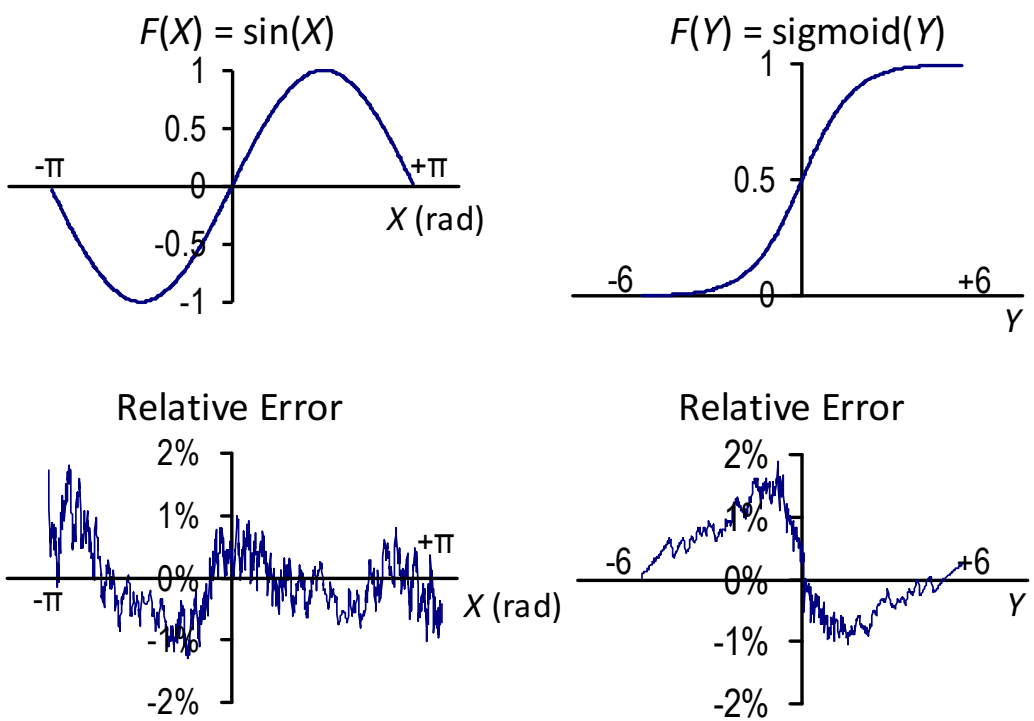
*Measurement conditions listed in Digest paper

Calibration helps improve accuracy

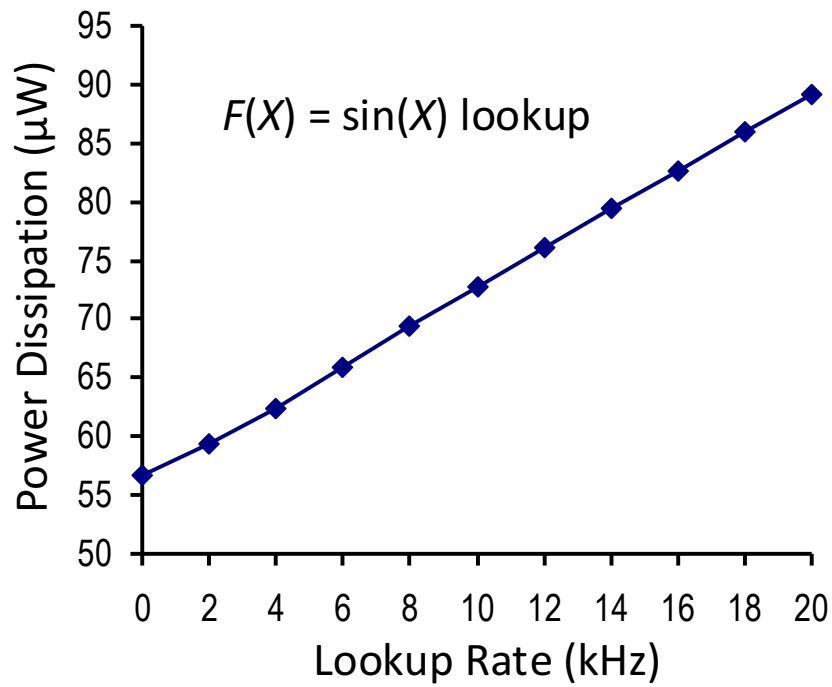
Nonlinear differential equation	RMS error (uncalibrated)	RMS error (calibrated)
Van der Pol oscillator	17.7%	1.9%
Large angle motion of pendulum	7.3%	1.5%
Mass-spring dampers with Coulomb friction	18.0%	1.5%

Measurement results

Nonlinear function generation:

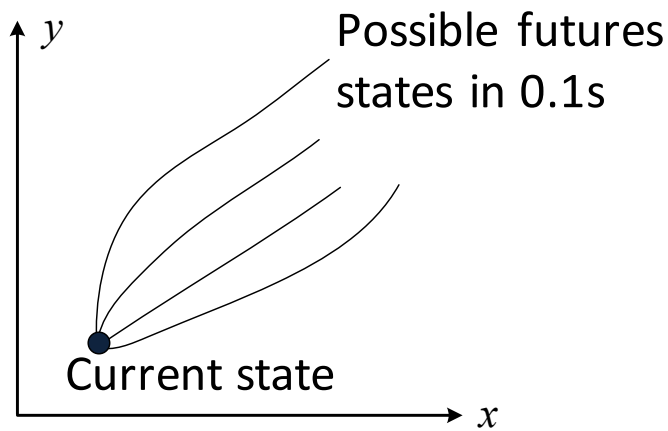


Activity-dependent power dissipation:



Application demonstration

A two-wheel drive robot with model predictive control



Continuous-time
system dynamics

$$\begin{aligned} \dot{x} &\quad \cos \\ \dot{y} &= \quad \sin \\ \dot{} & \end{aligned}$$

ω: angular velocity

v: linear velocity

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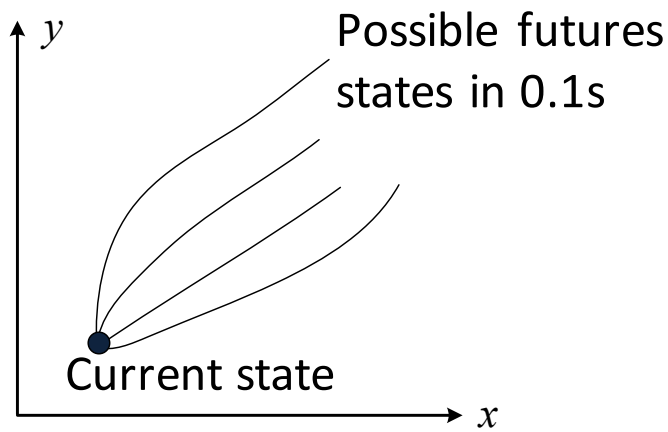
A two-wheel drive robot with model predictive control



Continuous-time system dynamics

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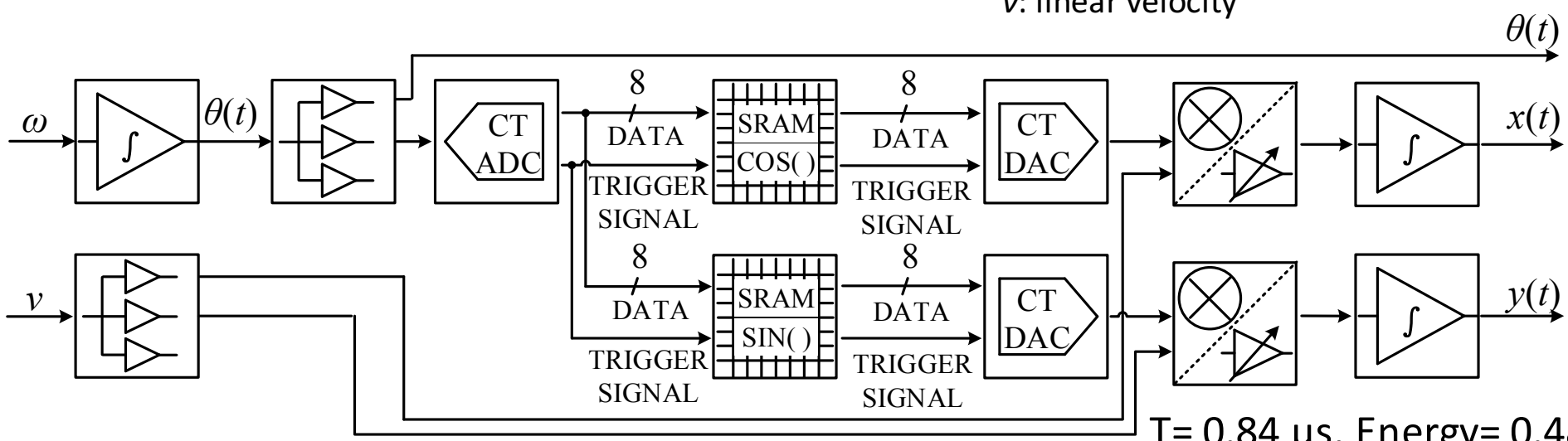

T= 0.84 µs, Energy= 0.48 nJ

RMS error = 0.6%

Comparison to prior art

	One macro in [1]	**Our chip**
Supply voltage	2.5 V	1.2V
Technology	250nm CMOS	65nm CMOS
Active area (estimate)	6.3 mm^2	2.0 mm^2
Number of function blocks	25	26
Power with all blocks on (estimate)	18.8 mW	**1.2 mW**
Calibration	Integrators only	**All blocks**
Computation types	CT analog only	CT analog / **CT hybrid**
Nonlinearities available for computation	Specific types: exp(), log(), absolute, saturation, etc.	**Arbitrary**
On-chip ADC, SRAM, DAC	N/A	Available

[1] G. Cowan et al., ISSCC 2005

Conclusions

- We have presented the first continuous-time hybrid computing unit.
- Arbitrary nonlinear functions are implemented by a continuous-time hybrid architecture (ADC+SRAM+DAC).
- We have used the chip to successfully solve several benchmark equations and demonstrated the use of the chip in a robotic application.
- We expect this technique to find applications in low-power approximate computation and in acceleration of digital computation.

Acknowledgement

We thank Chien-Tang Hu, Doyun Kim, Jianxun Zhu, Teng Yang, Yang Xu, Yu Chen and Zhe Cao for valuable discussions.

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References

[1]G. Cowan, R. Melville, and Y. Tsividis, “A VLSI analog computer / math co-processor for a digital computer”, Digest IEEE 2005 ISSCC, pp. 82-83.

[2] B. Schell and Y. Tsividis, “A clockless ADC/DSP/DAC system with activity-dependent power dissipation and no aliasing”, Digest 2008 IEEE ISSCC, pp. 550-551

[3] D. Kim et al., “A 1.85 fW/bit ultra low leakage 10T SRAM with speed compensation scheme”, Proc. IEEE ISCAS, pp. 69-72, May 2011.

[4] G. Klancar and I. Skrjanc, "Tracking-error model-based predictive control for mobile robots in real time," Robotics and Autonomous Systems, vol. 55, no. 6, pp. 460-469, 2007.

[6] G.A. Korn, T.M. Korn, *Electronic Analog and Hybrid Computers*, McGraw Hill, 1964.

[7] B. Gilbert, "Current-mode, voltage-mode, or free mode? A few sage suggestions”, Analog Integrated Circuits and Signal Processing, vol. 38, pp. 83-101, February 2004

Thank you!

Questions?

Comparison details

	Time step size	Total clock cycles	Time needed for one solution	Energy consumption for one solution
Our hybrid chip	N/A	N/A	0.84µs	0.48nJ
0.4V RISC microprocessor [8]	0.1s	734	29µs	5.14nJ

35X better **11X better**

[8] D. Bol, et al, "SleepWalker: A 25-MHz 0.4-V Sub-mm^2 7-µW/MHz Microcontroller in 65-nm LP/GP CMOS for Low-Carbon Wireless Sensor Nodes", IEEE JSSC, vol. 48, pp. 20-32, 2013.