Design of a Three-Stage High-Bandwidth CMOS Transimpedance Amplifier

Yipeng Huang
Department of Computer Science
Columbia University
yipeng@cs.columbia.edu

Jun Yin
Department of Electrical Engineering
Columbia University
jy2525@columbia.edu

***Abstract*—This report describes the development of a transimpedance amplifier that takes current as input and gives voltage as output. The amplifier consists of three CMOS amplifier stages in a fed-back configuration, achieving a transimpedance gain over 3 kΩ and a 3-dB bandwidth greater than 2.8 GHz. The amplifier operates with a 1.5 V supply voltage and a power budget of 30 mW.**

I. INTRODUCTION

A. TIA Applications in Fiber Optics Receivers

Photodiodes that are used in fiber optics receivers output signals at a high output impedance, therefore current mode signal transmission to the amplifier circuit is desirable (Fig. 1). The input source is a photodiode that gives a current as output, with two parasitic capacitances, the reverse-biased photodiode (C_{PD}), and the capacitance of the bond pad (C_{PAD}) (Fig. 2). We drive a 50 fF load at the output.

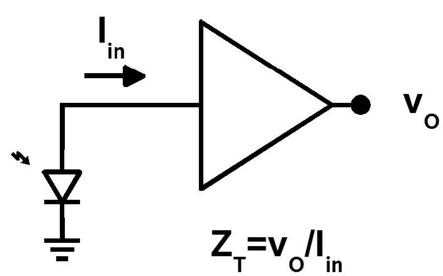

Fig. 1. Transimpedance amplifier as a photodiode signal amplifier.

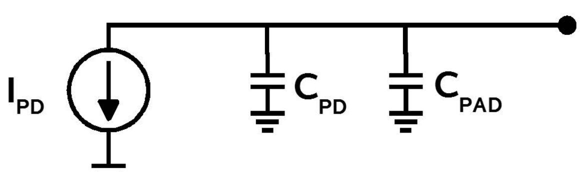

Fig. 2. The photodiode signal source comes with associated capacitances.

B. Design Targets

Table 1 outlines the specifications for this amplifier design.

TABLE I. AMPLIFIER SPECIFICATIONS

Specification	Target	Maximize Gain	Minimize Power
Transimpedance gain	> 3 kΩ (69.5 dB)	5.1 kΩ (74.2 dB) - 6.5 kΩ (76.2 dB)	3.6 kΩ (71.2 dB) - 4.7 kΩ (73.5 dB)
3-dB bandwidth	2.8 GHz		
Maximum current for linear operation	300 μA_{pp}		
Group delay variation	< 40 ps	20 ps	39 ps
Input resistance	Minimize	55 Ω	55 Ω
Output resistance	Minimize	109 Ω	354 Ω
Load capacitance	50 fF		
Supply voltage	1.5 V nominal, with 10% variation		
Reference current	50 µA available	Reference current not used	Reference current not used
Power consumption	< 30 mW	< 19 mW	< 15 mW
Operating temperature	-40 °C, 27 °C, 125 °C		

We present specifications for two designs that meet the target, one that maximizes gain, and the other minimizing power consumption. The third stage of the amplifier consumes most of the power, so decreasing its output voltage swing significantly improves over power consumption. The minimum power design consumes 14.6 mW at maximum when the amplifier is driven with a 1.333 GHz square wave input.

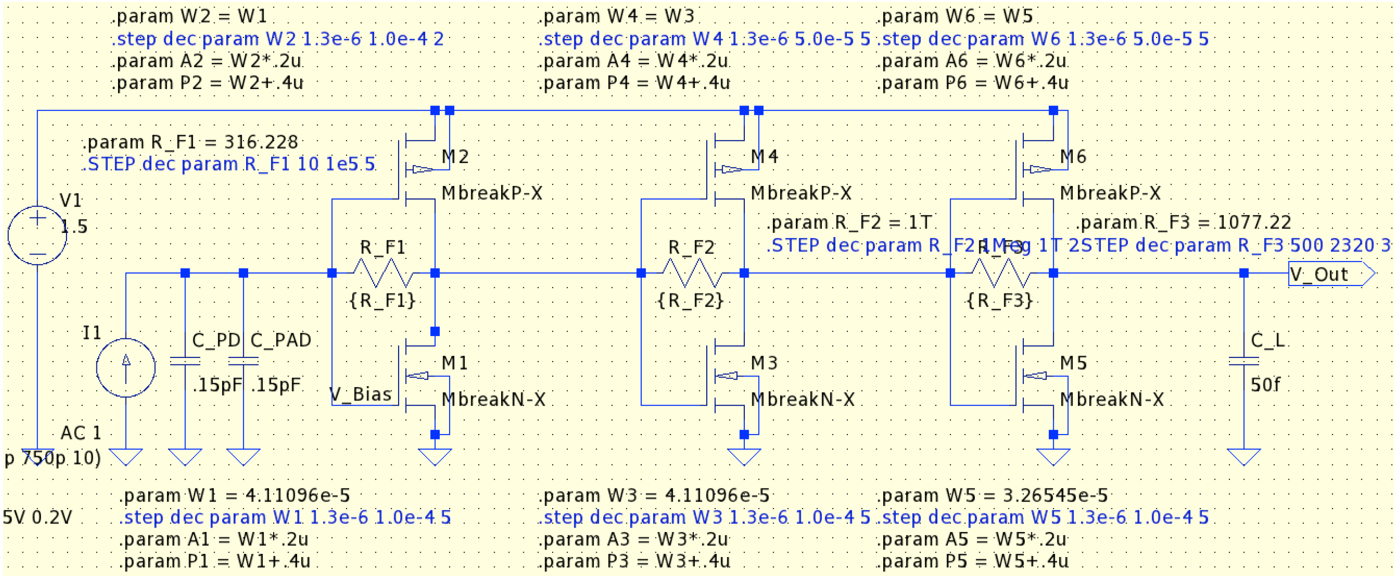

Fig. 3. The final circuit diagram.

II. Circuit Design

A. Candidate Designs

Several circuits were tested before choosing the final design. These included single-stage amplifiers with feedback, in both common source and CMOS inverter configurations. Both designs obtained 47 dB of gain while maintaining 3-dB bandwidth of 2.8 GHz. We noted the inverter configuration is more power efficient. A dual-stage design of the inverter configuration developed 60 dB of gain.

To get high gain, we tested cascode with feedback amplifier circuits. The single cascode achieved 70 dB, but could not keep this value for a 2.8 GHz bandwidth.

B. Final Design Description

The final design has three stages of the same layout (Fig. 3). In each stage, a pair of matched PMOS and NMOS transistors share the gate and the drain, as seen in CMOS inverter amplifier designs. To avoid the body effect, the body all devices are connected to their sources. A feedback resistor connects the each stages' output to its input. In the following sections, we discuss specific design issues.

TABLE II. Component Parameters

	First stage	**Second stage**	**Third stage**
Device width	41.1 μm	41.1 μm	8.2 μm
Device length	.13 μm	.13 μm	.13 μm
Feedback resistance	316 Ω	infinite	1,077 Ω
Bias point	612.5 mV	610 mV	600 mV
Gain	48 dB	13 dB	11 dB

C. Feedback Design

The feedback resistors serve different purposes in each stage. In the first stage, the shunt-shunt feedback resistor sets the bias voltage for the transistors, and decreases the input resistance, while trading gain for bandwidth at the same time. The second stage is purely a power amplifier; it calls for a feedback resistor with high resistance, and in fabrication simply no resistor would be present. The feedback resistor in the third stage serves to decrease the output resistance while again trading gain for bandwidth.

D. Process Technology

The transistors in our design have the parameters

$$0.13\ \mu m < L$$

$$0.13\ \mu m < W < 100\ \mu m$$

The source and drain areas AS = AD = W * 0.2 μm, and the source and drain perimeters PD = PS = W + 0.4 μm. The threshold voltage V_T = .332 V.

Our design uses purely minimum channel length devices, since channel length was not available initially as a design parameter. Incorporating longer length devices opens opportunity for meeting the requirements at even lower power consumption, or with additional leeway to accommodate process variations.

The high gain and high bandwidth of this design relies on perfect matching of the PMOS and NMOS devices in each stage. Imperfect matching leads to reduced gain in each stage and shifts the bias point for the transistors in the next stage. Realistic fabrication processes do not guarantee such perfect matching. Therefore, our design would incorporate DC blocking capacitors and level shifters in order to exert more control over the biasing of transistors.

E. CMOS Logic Design

Our design draws upon the CMOS inverter configuration, which can be used as an efficient amplifier for photodiode signals. In a CMOS inverter, the upper PMOS acts as a pull up device while the lower NMOS acts as an NMOS device. Drain current ID does not flow continuously, therefore conserving power.

F. Differential Mode Design

Our amplifier does not have a differential amplifier input stage, because our input is assumed not to be in differential mode. Realistic IC environments rely on differential mode circuitry to combat common mode noise from adjacent circuitry. An improvement on our design would incorporate a differential input stage.

III. Performance Derivations

In this section we derive key metrics of the amplifier.

A. Gain

From simulation we measure that the intrinsic gain A_0 of each inverter pair is about 1500 V/V. However, for stages with feedback resistors, the gain with feedback A_f is determined by the feedback network:

$$A_f = 1 / \beta = -R_f.$$

B. Output resistance

The output resistance without feedback of the third stage is determined by

$$R_o = (r_{o5} \| r_{o6}) = V_A' * L / 2 I_D$$

where V_A' is about 5.5 V/μm for 130 nm CMOS [1], and measured results show V_A = .54 V. We are able to measure I_D = .72 mA for the third stage designed for minimum power and find R_o = 497 Ω. However, the output resistance with feedback will be lower:

$$R_{of} = R_o / (1 + A_0\beta) = 357\ \Omega$$

which matches the simulation results.

C. Maximum output voltage swing

Given a maximum input current for linear operation of 300 μA, a tolerance of 1 dB lower than nominal gain at maximum input current, and a target transimpedance gain of 3 kΩ, the maximum output voltage is 300 μA * .8913 * 3 KΩ = .8021 V.

The maximum output voltage is constrained by the power supply voltage, which has a nominal value of 1.5 V, but can be as low as 1.35 V. We see that 1.35 V - .8021 V = .5479 V, which is some headroom to accommodate for V_{DS} drops.

IV. Simulation Results

In this section we present simulation results for the design that minimizes power consumption. Each plot will have multiple traces, each representing a different operation condition. Both temperature and voltage supply are swept across the required ranges.

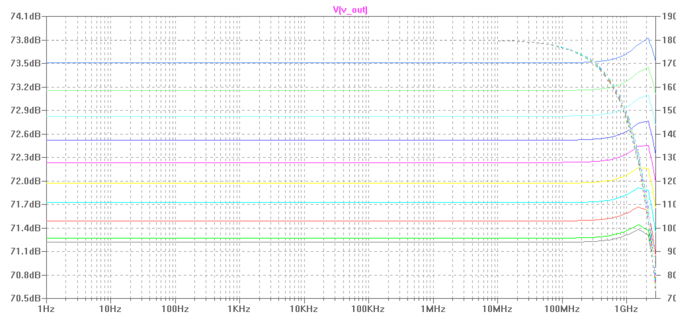

Fig. 4. Gain phase plot. The solid lines represent gain, which is kept above the desired 70 dB. The dashed lines represent phase shift, which stay within 180 degrees to prevent positive feedback.

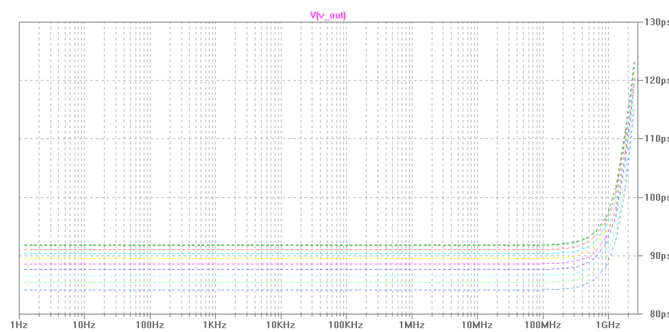

Fig. 5. Group delay plot. Group delay variation is kept within 40 ps across the 2.8 GHz operating bandwidth and across temperature and voltage supply variations.

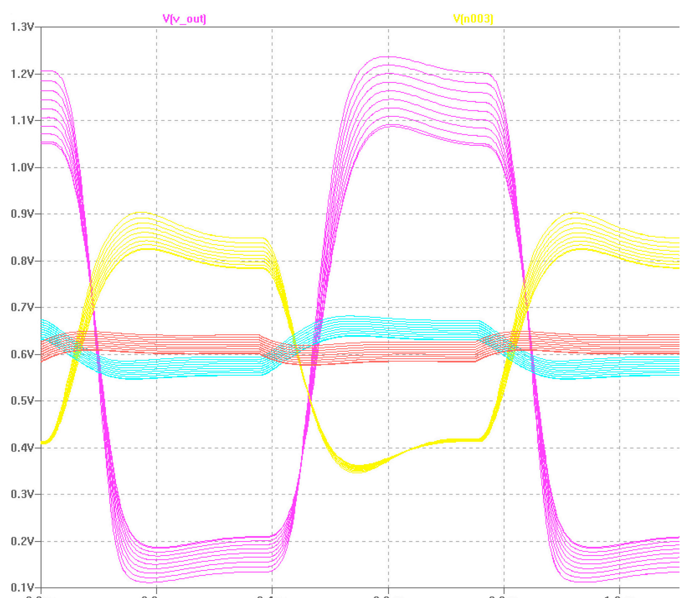

Fig. 6. Amplifier stages inputs outputs. We drive the amplifier with a 1.333 GHz, 300 μA_{pp} square wave to simulate operation with a photodiode input. Each plot with successively greater amplitude represents the output of each successive stage.

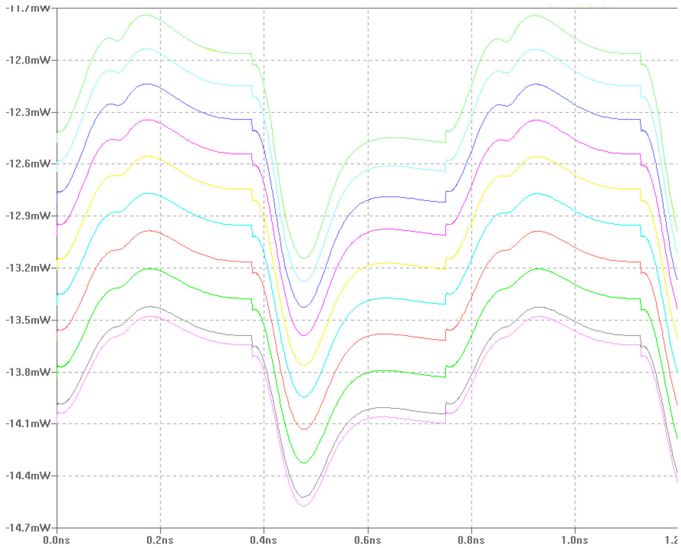

Fig. 7. Power consumption. Continuing with the inputs used in Fig. 6, we measure the power dissipation at the voltage supply. The peak power dissipation is 14.6 mW across the 2.8 GHz operating bandwidth and across temperature and voltage supply variations.

V. Conclusion

This report presents a transimpedance amplifier that uses multi-stage design, feedback, and CMOS inverter design to achieve a large transimpedance gain of over 3 kΩ over a wide 3-dB bandwidth of 2.8 GHz. The amplifer consumes less than 15 mW of power, and maintains its properties over a range of temperatures and supply voltages.

VI. References

[1] A. Sedra and K. Smith, Microelectronic Circuits, 6th ed. Oxford University Press, 2011. p 530.

[2] Paillet, Fabrice, and Tanay Karnik. High Gain, High Bandwidth CMOS Transimpedance Amplifier. Intel Corporation (Santa Clara, CA), assignee. Patent 6828857. 7 Dec. 2004.

VII. Appendix: SPICE Netlist

```
*
C:\users\yipenghuang0302\Testbench\Design_6_Detuned_Triple_Stage_Common_Sour
ce_Class_B.asc
C_PD V_Bias 0 .15pF
C_PAD V_Bias 0 .15pF
I1 0 V_Bias AC 1
M1 N002 V_Bias 0 0 MbreakN-X l=1.3e-7 w={W1} ad={A1} as={A1} pd={P1} ps={P1}
m=1
M2 N001 V_Bias N002 N001 MbreakP-X l=1.3e-7 w={W2} ad={A2} as={A2} pd={P2}
ps={P2}
R_F1 N002 V_Bias {R_F1}
C_L V_Out 0 50f
V1 N001 0 1.5
M4 N001 N002 N003 N001 MbreakP-X l=1.3e-7 w={W4} ad={A4} as={A4} pd={P4}
ps={P4}
M3 N003 N002 0 0 MbreakN-X l=1.3e-7 w={W3} ad={A3} as={A3} pd={P3} ps={P3}
m=1
R_F2 N002 N003 {R_F2}
M6 N001 N003 V_Out N001 MbreakP-X l=1.3e-7 w={W6} ad={A6} as={A6} pd={P6}
ps={P6}
M5 V_Out N003 0 0 MbreakN-X l=1.3e-7 w={W5} ad={A5} as={A5} pd={P5} ps={P5}
m=1
R_F3 N003 V_Out {R_F3}
.model NMOS NMOS
.model PMOS PMOS
.lib C:\Program Files\LTC\LTspiceIV\lib\cmp\standard.mos
.STEP TEMP -40 125 20
.STEP PARAM V_Supply 1.35V 1.75V 0.2V
;tran 0 2ns 0 .5ps
*
* Predictive Technology Model Beta Version
* 0.13um NMOS SPICE Parametersv (normal one)
*

.model MbreakN-X NMOS
+Level = 7

+Lint = 2.5e-08 Tox = 3.3e-09
+Vth0 = 0.332 Rdsw = 200

+lmin=1.3e-7 lmax=1.3e-7 wmin=1.3e-7 wmax=1.0e-4 Tnom=27.0
+Xj= 4.5000000E-08          Nch= 5.6000000E+17
+lln= 1.0000000             lwn= 0.00                  wln= 0.00
+wwn= 1.0000000             ll= 0.00
+lw= 0.00                   lwl= 0.00                  wint= 0.00
+wl= 0.00                   ww= 0.00                   wwl= 0.00
+Mobmod= 1                  binunit= 2
+Dwg= 0.00                  Dwb= 0.00

+K1= 0.3661500               K2= 0.00
+K3= 0.00                   Dvt0= 8.7500000            Dvt1= 0.7000000
+Dvt2= 5.0000000E-02        Dvt0w= 0.00                Dvt1w= 0.00
+Dvt2w= 0.00                Nlx= 3.5500000E-07         W0= 0.00
+K3b= 0.00                  Ngate= 5.0000000E+20

+Vsat= 1.3500000E+05        Ua= -1.8000000E-09         Ub= 2.2000000E-18
+Uc= -2.9999999E-11         Prwb= 0.00
+Prwg= 0.00                 Wr= 1.0000000              U0= 1.3400000E-02
+A0= 2.1199999              Keta= 4.0000000E-02        A1= 0.00
+A2= 0.9900000              Ags= -0.1000000            B0= 0.00
+B1= 0.00

+Voff= -7.9800000E-02       NFactor= 1.1000000         Cit= 0.00
+Cdsc= 0.00                 Cdscb= 0.00                Cdscd= 0.00
+Eta0= 4.0000000E-02        Etab= 0.00                 Dsub= 0.5200000

+Pclm= 0.1000000            Pdiblc1= 1.2000000E-02     Pdiblc2= 7.5000000E-03
+Pdiblcb= -1.3500000E-02    Drout= 0.2800000           Pscbe1= 8.6600000E+08
+Pscbe2= 1.0000000E-20      Pvag= -0.2800000           Delta= 1.0100000E-02
+Alpha0= 0.00               Beta0= 30.0000000

+kt1= -0.3400000            kt2= -5.2700000E-02        At= 0.00
+Ute= -1.2300000            Ua1= -8.6300000E-10        Ub1= 2.0000001E-18
+Uc1= 0.00                  Kt1l= 4.0000000E-09        Prt= 0.00

+Cj= 0.0015                 Mj= 0.7175511              Pb= 1.24859
+Cjsw= 2E-10                Mjsw= 0.3706993            Pbsw= 0.7731149
+         JS=2.50E-08                 JSW=4.00E-13
+N=1.0                      Xti=3.0                    Cgdo=2.75E-10
+Cgso=2.75E-10              Cgbo=0.0E+00               Capmod= 2
+NQSMOD= 0                  Elm= 5                     Xpart= 1
+Cgsl= 1.1155E-10           Cgdl= 1.1155E-10           Ckappa= 0.8912
+Cf= 1.113e-10              Clc= 5.475E-08             Cle= 6.46
+Dlc= 2E-08                 Dwc= 0                     Vfbcv= -1

*
* Predictive Technology Model Beta Version
* 0.13um PMOS SPICE Parametersv (normal one)
*

.model MbreakP-X PMOS
+Level = 7

+Lint = 2.e-08 Tox = 3.3e-09
+Vth0 = -0.3499 Rdsw = 400

+lmin=1.3e-7 lmax=1.3e-7 wmin=1.3e-7 wmax=1.0e-4 Tnom=27.0
+Xj= 4.5000000E-08          Nch= 6.8500000E+18
+lln= 0.00                  lwn= 0.00                  wln= 0.00
+wwn= 0.00                  ll= 0.00
+lw= 0.00                   lwl= 0.00                  wint= 0.00
+wl= 0.00                   ww= 0.00                   wwl= 0.00
+Mobmod=  1                 binunit= 2
+
+Dwg= 0.00                  Dwb= 0.00

+K1= 0.4087000              K2= 0.00
+K3= 0.00                   Dvt0= 5.0000000            Dvt1= 0.2600000
+Dvt2= -1.0000000E-02       Dvt0w= 0.00                Dvt1w= 0.00
+Dvt2w= 0.00                Nlx= 1.6500000E-07         W0= 0.00
+K3b= 0.00                  Ngate= 5.0000000E+20

+Vsat= 1.0500000E+05        Ua= -1.4000000E-09         Ub= 1.9499999E-18
+Uc= -2.9999999E-11         Prwb= 0.00
+Prwg= 0.00                 Wr= 1.0000000              U0= 5.2000000E-03
+A0= 2.1199999              Keta= 3.0300001E-02        A1= 0.00
+A2= 0.4000000              Ags= 0.1000000             B0= 0.00
+B1= 0.00

+Voff= -9.10000000E-02      NFactor= 0.1250000         Cit= 2.7999999E-03
+Cdsc= 0.00                 Cdscb= 0.00                Cdscd= 0.00
+Eta0= 80.0000000           Etab= 0.00                 Dsub= 1.8500000

+Pclm= 2.5000000            Pdiblc1= 4.8000000E-02     Pdiblc2= 5.0000000E-05
+Pdiblcb= 0.1432509         Drout= 9.0000000E-02       Pscbe1= 1.0000000E-20
+Pscbe2= 1.0000000E-20      Pvag= -6.0000000E-02       Delta= 1.0100000E-02
+Alpha0= 0.00               Beta0= 30.0000000

+kt1= -0.3400000            kt2= -5.2700000E-02        At= 0.00
+Ute= -1.2300000            Ua1= -8.6300000E-10        Ub1= 2.0000001E-18
+Uc1= 0.00                  Kt1l= 4.0000000E-09        Prt= 0.00

+Cj= 0.0015                 Mj= 0.7175511              Pb= 1.24859
+Cjsw= 2E-10                Mjsw= 0.3706993            Pbsw= 0.7731149
+Cta= 9.290391E-04          Ctp= 7.456211E-04          Pta= 1.527748E-03
+Ptp= 1.56325E-03           JS=2.50E-08                JSW=4.00E-13
+N=1.0                      Xti=3.0                    Cgdo=2.75E-10
+Cgso=2.75E-10              Cgbo=0.0E+00               Capmod= 2
+NQSMOD= 0                  Elm= 5                     Xpart= 1
+Cgsl= 1.1155E-10           Cgdl= 1.1155E-10           Ckappa= 0.8912
+Cf= 1.113e-10              Clc= 5.475E-08             Cle= 6.46
+Dlc= 2E-08                 Dwc= 0                     Vfbcv= -1
.ac oct 2 1 2.8G
* .STEP dec param R_F1 10 1e5 5
.param W2 = W1
* .step dec param W2 1.3e-6 1.0e-4 2
.param A2 = W2*.2u
.param P2 = W2+.4u
.param R_F1 = 316.228
.param W1 = 4.11096e-5
* .step dec param W1 1.3e-6 1.0e-4 5
.param A1 = W1*.2u
.param P1 = W1+.4u
.param W4 = W3
* .step dec param W4 1.3e-6 5.0e-5 5
.param A4 = W4*.2u
.param P4 = W4+.4u
.param W3 = 4.11096e-5
* .step dec param W3 1.3e-6 1.0e-4 5
.param A3 = W3*.2u
.param P3 = W3+.4u
* .STEP dec param R_F2 1Meg 1T 2
.param R_F2 = 1T
.param W6 = W5
* .step dec param W6 1.3e-6 5.0e-5 5
.param A6 = W6*.2u
.param P6 = W6+.4u
.param W5 = 8.20245e-6
* .step dec param W5 1.3e-6 1.0e-4 5
.param A5 = W5*.2u
.param P5 = W5+.4u
* .STEP dec param R_F3 500 2320 3
.param R_F3 = 1077.22
;tf V(V_Out) I1
.backanno
.end
```