Assembly: Introduction.

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Table of contents

Looking ahead

Class plan

1. Today, Tuesday, 2/23: Bits to oats. Introduction to the software-hardware interface.
2. Reading assignment for next four weeks: CS:APP Chapter 3.
3. Thursday, 2/25: Programming Assignment 3 on bits, bytes, integers, oats out.
4. Monday, 3/1: Programming Assignment 2 due. Be sure to test on ilab, "make clean". Quiz 6 on oating point trickiness out.

Table of contents

Floating point numbers

Avogadro's number

$+6.02214 \times 10^{23}\,\text{mol}^{-1}$

Scientific notation

- sign
- mantissa or significand
- exponent

Floats and doubles

Figure: The two standard formats for oating point data types. Image credit CS:APP

Floats and doubles

property	oat	double
total bits	32	64
s bit	1	1
exp bits	8	11
frac bits	23	52
C printf() format speci er	"%f"	"%lf"

Table: Properties of oats and doubles

The IEEE 754 number line

Figure: Full picture of number line for oating point values. Image credit CS:APP

Figure: Zoomed in number line for oating point values. Image credit CS:APP

Different cases for floating point numbers

Value of the floating point number = $(-1)^s \times M \times 2^E$

- E is encoded the exp field
- M is encoded the frac field

Figure: Different cases within a floating point format. Image credit CS:APP

Normalized and denormalized numbers

Two different cases we need to consider for the encoding of E, M

Normalized: exp eld

For normalized numbers,
$0 < \text{exp} < 2^k$ 1

- exp is a k-bit unsigned integer

Bias

- need a bias to represent negative exponents
- bias = 2^{k} 1 1
- bias is the k-bit unsigned integer: 011..111

For normalized numbers,
E = exp-bias

In other words, exp = E+bias

property	oat	double
k	8	11
bias	127	1023
smallest E (greatest precision)	-126	-1022
largest E (greatest range)	127	1023

Table: Summary of normalized exp eld

Normalized: frac eld

M = 1.frac

Floats: Summary

	normalized	denormalized
value of number	$(-1)^s \times M \times 2^E$	$(-1)^s \times M \times 2^E$
E	E = exp-bias	E = -bias + 1
bias	$2^{k-1} - 1$	$2^{k-1} - 1$
exp	$0 < exp < (2^k - 1)$	exp= 0
M	M = 1.frac	M = 0.frac
	M has implied leading 1	M has leading 0
	greater range	greater precision
	large magnitude numbers	small magnitude numbers
	denser near origin	evenly spaced

Table: Summary of normalized and denormalized numbers

Floats: Special cases

number class	when it arises	exp eld	frac eld
+0 / -0		0	0
+in nity / -in nity	over ow or division by 0	2^k 1	0
NaN not-a-number	illegal ops. such as $\sqrt{\ 1}$, inf-inf, inf*0	2^k 1	non-0

Table: Summary of special cases

Table of contents

Normalized number bitstring to real number it represents

- Tiny FP: 1-bit s, 4-bit exp, 3-bit frac
- What does this encode: 1_1001_101
- s=1, so positive? negative?
- exp = 1001_2
- bias = $2^{k\quad 1}\quad 1 = 2^{4\quad 1}\quad 1 = 7$
- E = exp-bias =
- frac = 101_2
- M = 1.frac = $1{:}101_2$

How to multiply scienti c notation?

Recall: $\log(x \quad y) = \log(x) + \log(y)$

Floating point multiplication

Properties of oating point

Properties of oating point

Table of contents

Computer organization

Layer cake

- Society
- Human beings
- Applications
- Algorithms
- High-level programming languages
- Interpreters
- Low-level programming languages
- Compilers
- Architectures
- Microarchitectures
- Sequential/combinational logic
- Transistors
- Semiconductors
- Materials science

why are instruction set architectures important

Interface between computer science and electrical and computer engineering

- Software is varied, changes
- Hardware is standardized, static

Computer architect Fred Brooks and the IBM 360

- IBM was selling computers with different capacities,
- Compile once, and can run software on all IBM machines.
- Backward compatibility.
- An in uential idea.

CISC vs. RISC

Complex instruction set computer

- Intel and AMD
- Have an extensive and complex set of instructions
- For example: x86's extensions: x87, IA-32, x86-64, MMX, 3DNow!, SSE, SSE2, SSE3, SSSE3, SSE4, SSE4.2, SSE5, AES-NI, CLMUL, RDRAND, SHA, MPX, SGX, XOP, F16C, ADX, BMI, FMA, AVX, AVX2, AVX512, VT-x, VT-d, AMD-V, AMD-Vi, TSX, ASF
- Can license Intel's compilers to extract performance
- Secret: inside the processor, they break it down to more elementary instructions

CISC vs. RISC

Reduced instruction set computer

- MIPS, ARM, RISC-V (can find Patterson and Hennessy Computer Organization and Design textbook in each of these versions), an PowerPC
- Have a relatively simple set of instructions
- For example: ARM's extensions: SVE;SVE2;TME; All mandatory: Thumb-2, Neon, VFPv4-D16, VFPv4 Obsolete: Jazelle
- ARM: smartphones, Apple ARM M1 Mac