

# Machine-level representation of programs: Bomblab, addressing mode recap, arithmetic

Yipeng Huang

Rutgers University

March 22, 2022

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# Announcements

## PA4 bomb lab

- ▶ PA4 bomb lab out and live. Due Tuesday, April 5.
- ▶ Due dates for rest of semester up to date on class syllabus.  
<https://yipenghuang.com/teaching/2022-spring/>

## Short quiz next week

Short quiz on assembly basics and control spanning Tuesday 3/29 to Thursday 3/31.

## Class session plan

- ▶ Today, 3/22: Bomb lab demo, recap addressing modes, wrap up arithmetic.
- ▶ Thursday, 3/24: Control flow (conditionals, if, for, while, do loops) in assembly. (Book chapter 3.6)
- ▶ Tuesday, 3/29: Function calls in assembly. (Book chapter 3.7)
- ▶ Thursday, 3/31: Arrays and data structures in assembly. (Book chapter 3.8)

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# Programming Assignment 4: Defusing a Binary Bomb

## Goals

- ▶ Learning to learn to use important tools like GDB.
- ▶ Understand how high level programming constructs compile down to assembly instructions.
- ▶ Practice reverse engineering and debugging.

## Setup

- ▶ Programming assignment description PDF on Canvas.
- ▶ Web interface for obtaining bomb and seeing progress.
- ▶ Unpacking.

# Unpacking and gathering information about your bomb

## What comes in the package

- ▶ `bomb.c`: Skeleton source code
- ▶ `bomb`: The executable binary

```
objdump -t bomb > symbolTable.txt
```

- ▶ `000000000040143a g F .text 0000000000000022 explode_bomb`

```
objdump -d bomb > bomb.s
```

Different phases correspond to different topics about assembly programming in the CS211 lecture slides, in the CS:APP slides, and in the CS:APP book.

- ▶ `phase_1`
- ▶ `phase_2`
- ▶ `explode_bomb`

```
strings -t x bomb > strings.txt
```

## Example phase\_1 in example bomb from CS:APP website

```
0000000000400ee0 <phase_1>:
 400ee0: 48 83 ec 08          sub     $0x8,%rsp
 400ee4: be 00 24 40 00      mov     $0x402400,%esi
 400ee9: e8 4a 04 00 00     callq  401338 <strings_not_equal>
 400eee: 85 c0              test   %eax,%eax
 400ef0: 74 05             je     400ef7 <phase_1+0x17>
 400ef2: e8 43 05 00 00     callq  40143a <explode_bomb>
 400ef7: 48 83 c4 08       add     $0x8,%rsp
 400efb: c3              retq
```

### Understanding what we're seeing here

- ▶ Don't let `callq` to `explode_bomb` at instruction address `400ef2` happen...
- ▶ so, must ensure `je` instruction does jump, so we want `test` instruction to set ZF condition code to 0.
- ▶ so, must ensure `callq` to `strings_not_equal()` function returns 0.

# Using GDB to carefully step through execution of the bomb program

```
gdb bomb
```

## Finding help in GDB

- ▶ `help`: Menu of documentation.
- ▶ `help layout`: Useful tip to use either `layout asm` or `layout regs` for this assignment.
- ▶ `help aliases`
- ▶ `help running`
- ▶ `help data`
- ▶ `help stack`



# Using GDB to carefully step through execution of the bomb program

```
gdb bomb
```

## Setting breakpoints and running / stepping through code

- ▶ `break explode_bomb` or `b explode_bomb`: Pause execution upon entering `explode_bomb` function.
- ▶ `break phase_1` or `b phase_1`: Pause execution upon entering `phase_1` function.
- ▶ `run mysolution.txt` or `r mysolution.txt`: Run the code passing the solution file.
- ▶ `continue` or `c`: Continue until the next breakpoint.
- ▶ `nexti` or `ni`: Step one instruction, but proceed through subroutine calls.
- ▶ `stepi` or `si`: Step one instruction exactly. Steps into functions / subroutine calls.

# Using GDB to carefully step through execution of the bomb program

```
gdb bomb
```

## Printing and examining registers and memory addresses

- ▶ `print /x $eax` or `p /x $eax`: Print value of `%eax` register as hex.
- ▶ `print /d $eax` or `p /d $eax`: Print value of `%eax` register as decimal.
- ▶ `x /s 0x402400`: Examine memory address `0x402400` as a string.

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# Immediate, register, and memory

## Immediate

Constant integer values. Example: `2_addressing_modes.c` `immediate()`

## Register

One of the registers of appropriate size for data type. Example: `1_swap.c`

## Memory

Access to memory at calculated

## movq Operand Combinations

	Source	Dest	Src, Dest	C Analog
movq	Imm	Reg	<code>movq \$0x4, %rax</code>	<code>temp = 0x4;</code>
		Mem	<code>movq \$-147, (%rax)</code>	<code>*p = -147;</code>
	Reg	Reg	<code>movq %rax, %rdx</code>	<code>temp2 = temp1;</code>
		Mem	<code>movq %rax, (%rdx)</code>	<code>*p = temp;</code>
	Mem	Reg	<code>movq (%rax), %rdx</code>	<code>temp = *p;</code>

**Cannot do memory-memory transfer with a single instruction**

## Simple Memory Addressing Modes

### ■ Normal (R) Mem[Reg[R]]

- Register R specifies memory address
- Aha! Pointer dereferencing in C

```
movq (%rcx), %rax
```

### ■ Displacement D(R) Mem[Reg[R]+D]

- Register R specifies start of memory region
- Constant displacement D specifies offset

```
movq 8(%rbp), %rdx
```

## Normal

Simple pointers.

Example: 2\_addressing\_modes.c  
immediate()

## Displacement

Array access with constant index.

Example: 2\_addressing\_modes.c  
displacement()

## Complete Memory Addressing Modes

### ■ Most General Form

$D(Rb, Ri, S)$                        $Mem[Reg[Rb]+S*Reg[Ri]+ D]$

- D: Constant “displacement” 1, 2, or 4 bytes
- Rb: Base register: Any of 16 integer registers
- Ri: Index register: Any, except for `%rsp`
- S: Scale: 1, 2, 4, or 8 (*why these numbers?*)

### ■ Special Cases

$(Rb, Ri)$                                $Mem[Reg[Rb]+Reg[Ri]]$

$D(Rb, Ri)$                               $Mem[Reg[Rb]+Reg[Ri]+D]$

$(Rb, Ri, S)$                            $Mem[Reg[Rb]+S*Reg[Ri]]$

## Indexed

Array access with variable index.

Example: `2_addressing_modes.c`  
`index()`

## Address Computation Examples

<code>%rdx</code>	<code>0xf000</code>
<code>%rcx</code>	<code>0x0100</code>

Expression	Address Computation	Address
<code>0x8(%rdx)</code>	<code>0xf000 + 0x8</code>	<code>0xf008</code>
<code>(%rdx,%rcx)</code>	<code>0xf000 + 0x100</code>	<code>0xf100</code>
<code>(%rdx,%rcx,4)</code>	<code>0xf000 + 4*0x100</code>	<code>0xf400</code>
<code>0x80(,%rdx,2)</code>	<code>2*0xf000 + 0x80</code>	<code>0x1e080</code>

## 2\_addressing\_modes.c: Imm→Mem

### C code

```
void immediate ( long * ptr ) {  
    *ptr = 0xFFFFFFFFFFFFFFFF;  
}
```

### Assembly code

```
immediate:  
    movq $-1, (%rdi)  
    ret
```

- ▶ \$ indicates the immediate value; corresponds to literals in C
- ▶ (%rdi) indicates memory location at address stored in %rdi register



## 2\_addressing\_modes.c: Imm→Mem (with displacement)

### C code

```
void displacement_l ( long * ptr ) {  
    ptr[1] = 0xFFFFFFFFFFFFFFFF;  
}
```

- ▶ `8(%rdi)` indicates memory location at address stored in `%rdi` register + 8

### Assembly code

```
displacement_l:  
    movq $-1, 8(%rdi)  
    ret
```

## 2\_addressing\_modes.c: Imm→Mem (with displacement)

function signature	assembly code
<code>void displacement_c ( char * ptr );</code>	<code>movb \$-1, 1(%rdi)</code>
<code>void displacement_s ( short * ptr );</code>	<code>movw \$-1, 2(%rdi)</code>
<code>void displacement_i ( int * ptr );</code>	<code>movl \$-1, 4(%rdi)</code>
<code>void displacement_l ( long * ptr );</code>	<code>movq \$-1, 8(%rdi)</code>

## 2\_addressing\_modes.c: Imm→Mem (with index)

### C code

```
void index_l ( long * ptr, long index ) {  
    ptr[index] = 0xFFFFFFFFFFFFFFFF;  
}
```

- ▶ `(%rdi,%rsi,8)` indicates memory location at address stored in `%rdi` register +  $8 \times$  value stored in `%rsi` register

### Assembly code

```
index_l:  
    movq $-1, (%rdi,%rsi,8)  
    ret
```

## 2\_addressing\_modes.c: Imm→Mem (with index)

function signature	assembly code
<code>void index_c ( char * ptr, long index );</code>	<code>movb \$-1, (%rdi,%rsi)</code>
<code>void index_s ( short * ptr, long index );</code>	<code>movw \$-1, (%rdi,%rsi,2)</code>
<code>void index_i ( int * ptr, long index );</code>	<code>movl \$-1, (%rdi,%rsi,4)</code>
<code>void index_l ( long * ptr, long index );</code>	<code>movq \$-1, (%rdi,%rsi,8)</code>

## 2\_addressing\_modes.c: Imm→Mem (with displacement and index)

### C code

```
void displacement_and_index ( long * ptr, long index ) {  
    ptr[index+1] = 0xFFFFFFFFFFFFFFFF;  
}
```

- ▶ `8(%rdi,%rsi,8)` indicates memory location at address stored in `%rdi` register +  $8 \times$  value stored in `%rsi` register + 8

### Assembly code

```
displacement_and_index:  
    movq $-1, 8(%rdi,%rsi,8)  
    ret
```

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# 3\_leaq.s: Borrowing memory address calculation to efficiently implement arithmetic

## Address Computation Instruction

### ■ `leaq Src, Dst`

- Src is address mode expression
- Set Dst to address denoted by expression

### ■ Uses

- Computing addresses without a memory reference
  - E.g., translation of `p = &x[i];`
- Computing arithmetic expressions of the form  $x + k*y$ 
  - $k = 1, 2, 4, \text{ or } 8$

### ■ Example

```
long m12(long x)
{
    return x*12;
}
```

Converted to ASM by compiler:

```
leaq (%rdi,%rdi,2), %rax # t <- x+x*2
salq $2, %rax           # return t<<2
```

Example: 3\_leaq.c

# Load effective address

---

```
1 long * leaq (  
2     long * ptr, long index  
3 ) {  
4     return &ptr[index+1];  
5 }
```

---

```
1 long mulAdd (  
2     long base, long index  
3 ) {  
4     return base+index*8+8;  
5 }
```

---

Both C code functions above translate to the assembly on the right.

leaq:

mulAdd:

```
leaq 8(%rdi,%rsi,8), %rax  
ret
```

## Explanation

- ▶ `leaq src, dest` takes the effective address of the memory (index, displacement) expression of `src` and puts it in `dest`.
- ▶ `leaq` has shorter latency (takes fewer CPU cycles) than `imulq`, so GCC will use `leaq` whenever it can to calculate expressions like  $y + ax + b$ .



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# Sign extension due to unsigned and signed data types

## Converting to a data type with more bits

```
1 unsigned short uc_to_us (  
2     unsigned char input  
3 ) {  
4     return input;  
5 }
```

```
1 signed short sc_to_ss (  
2     signed char input  
3 ) {  
4     return input;  
5 }
```

$$\begin{aligned}255 &= 1111_1111_2 \\ &= 0000_0000_1111_1111_2 \\ &= 255\end{aligned}$$

$$\begin{aligned}127 &= 0111_1111_2 \\ &= 0000_0000_0111_1111_2 \\ &= 127\end{aligned}$$

$$\begin{aligned}-128 &= 1000_0000_2 \\ &= 1111_1111_1000_0000_2 \\ &= -128\end{aligned}$$

# Sign extension due to unsigned and signed data types

## Converting to a data type with more bits

---

```
1 unsigned short uc_to_us (  
2     unsigned char input  
3 ) {  
4     return input;  
5 }
```

---

---

```
1 signed short  sc_to_ss (  
2     signed char input  
3 ) {  
4     return input;  
5 }
```

---

function signature	assembly code
unsigned short uc_to_us ( unsigned char input );	movzbl %dil, %eax
signed short uc_to_ss ( unsigned char input );	movzbl %dil, %eax
unsigned short sc_to_us ( signed char input );	movsbw %dil, %ax
signed short sc_to_ss ( signed char input );	movsbw %dil, %ax

- ▶ movz: zero extension in the MSBs
- ▶ movs: signed extension in the MSBs

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# Left shift operation

---

```
1 unsigned long sl_ul (  
2     unsigned long in0,  
3     unsigned long in1  
4 ) {  
5     return in0<<in1;  
6 }
```

---

```
1 signed long sl_sl (  
2     signed long in0,  
3     signed long in1  
4 ) {  
5     return in0<<in1;  
6 }
```

---

Both C code functions above translate to the assembly on the right.

```
sl_ul:  
sl_sl:  
    movq %rdi, %rax  
    movb %sil, %cl  
    salq %cl, %rax  
    ret
```

## Explanation

- ▶ `movq: in0` → `%rdi` → `%rax`
- ▶ `movb: in1` → `%sil` → `%cl`
- ▶ `salq src, dest:`  
(`dest << src`) → `dest`
- ▶ Why only use `movb` for `in1`?

# Right shift operation

Right shift of unsigned types yields logical (zero-filled) right shift

---

```
1 unsigned long sr_ul (  
2     unsigned long in0,  
3     unsigned long in1  
4 ) {  
5     return in0>>in1;  
6 }
```

---

```
sr_ul:  
    movq %rdi, %rax  
    movb %sil, %cl  
    shrq %cl, %rax  
    ret
```

Right shift of signed types yields arithmetic (sign-extended) right shift

---

```
1 signed long sr_sl (  
2     signed long in0,  
3     signed long in1  
4 ) {  
5     return in0>>in1;  
6 }
```

---

```
sr_sl:  
    movq %rdi, %rax  
    movb %sil, %cl  
    sarq %cl, %rax  
    ret
```

# Bitwise operations

Assembly instruction	Instruction effect
<code>notq dest</code>	$\sim \text{dest} \rightarrow \text{dest}$
<code>andq src, dest</code>	$\text{src} \& \text{dest} \rightarrow \text{dest}$
<code>orq src, dest</code>	$\text{src}   \text{dest} \rightarrow \text{dest}$
<code>xorq src, dest</code>	$\text{src} \wedge \text{dest} \rightarrow \text{dest}$

# Integer arithmetic operations

Assembly instruction	Instruction effect
<code>incq dest</code>	$\text{dest} + 1 \rightarrow \text{dest}$
<code>decq dest</code>	$\text{dest} - 1 \rightarrow \text{dest}$
<code>negq dest</code>	$-\text{dest} \rightarrow \text{dest}$
<code>addq src, dest</code>	$\text{src} + \text{dest} \rightarrow \text{dest}$
<code>subq src, dest</code>	$\text{src} - \text{dest} \rightarrow \text{dest}$
<code>imulq src, dest</code>	$\text{src} \times \text{dest} \rightarrow \text{dest}$



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# What is control flow?

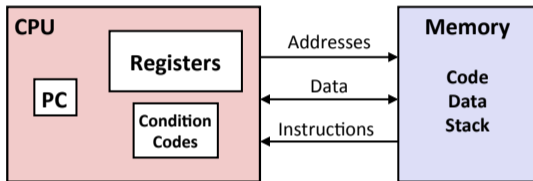
## Control flow is:

- ▶ Change in the sequential execution of instructions.
- ▶ Change in the steady incrementation of the program counter / instruction pointer (%rip register).

## Control primitives in assembly build up to enable C and Java control statements:

- ▶ if-else statements
- ▶ do-while loops
- ▶ while loops
- ▶ for loops
- ▶ switch statements

## Assembly/Machine Code View



### Programmer-Visible State

- **PC: Program counter**
  - Address of next instruction
  - Called "RIP" (x86-64)
- **Register file**
  - Heavily used program data
- **Condition codes**
  - Store status information about most recent arithmetic or logical operation
  - Used for conditional branching
- **Memory**
  - Byte addressable array
  - Code and user data
  - Stack to support procedures

## Condition codes

Automatically set by most arithmetic instructions.

Applicable types	Condition code	Name	Use
Signed and unsigned	ZF	Zero flag	The most recent operation yielded zero.
Unsigned types	CF	Carry flag	The most recent operation generated a carry out of the most significant bit. Used to detect overflow for unsigned operations
Signed types	SF	Sign flag	The most recent operation yielded a negative value.
Signed types	OF	Overflow flag	The most recent operation yielded a two's complement positive or negative overflow.

**Table:** Condition codes important for control flow

# Comparison instructions

```
cmpq source1, source2
```

Performs  $\text{source2} - \text{source1}$ , and sets the condition codes without setting any destination register.

# Test for equality

---

```
1 short equal_sl (  
2     long x,  
3     long y  
4 ) {  
5     return x==y;  
6 }
```

---

C code function above translates to the assembly on the right.

```
equal_sl:  
    xorl %eax, %eax  
    cmpq %rsi, %rdi  
    sete %al  
    ret
```

## Explanation

- ▶ `xorl %eax, %eax`: Zeros the 32-bit register `%eax`.
- ▶ `cmpq %rsi, %rdi`: Calculates  $\%rdi - \%rsi$  ( $x - y$ ), sets condition codes without updating any destination register.
- ▶ `sete %al`: Sets the 8-bit `%al` subset of `%eax` if op yielded zero.

# Test if unsigned x is below unsigned y

---

```
1 short below_ul (  
2     unsigned long x,  
3     unsigned long y  
4 ) {  
5     return x<y;  
6 }
```

---

```
1 short nae_ul (  
2     unsigned long x,  
3     unsigned long y  
4 ) {  
5     return !(x>=y);  
6 }
```

---

Both C code functions above translate to the assembly on the right.

```
below_ul:  
nae_ul:  
    xorl %eax, %eax  
    cmpq %rsi, %rdi  
    setb %al  
    ret
```

## Explanation

- ▶ `xorl %eax, %eax`: Zeros %eax.
- ▶ `cmpq %rsi, %rdi`: Calculates  $\%rdi - \%rsi$  ( $x - y$ ), sets condition codes without updating any destination register.
- ▶ `setb %al`: Sets %al if CF flag set indicating unsigned overflow.

## Side review: De Morgan's laws

▶  $\neg A \wedge \neg B \iff \neg(A \vee B)$

▶  $(\sim A) \& (\sim B) \iff \sim (A|B)$



## Set instructions

`cmp source1, source2` performs `source2 - source1`, sets condition codes.

Applicable types	Set instruction	Logical condition	Intuitive condition
Signed and unsigned	<code>sete / setz</code>	ZF	Equal / zero
Signed and unsigned	<code>setne / setnz</code>	$\sim$ ZF	Not equal / not zero
Unsigned	<code>setb / setnae</code>	CF	Below
Unsigned	<code>setbe / setna</code>	CF ZF	Below or equal
Unsigned	<code>seta / setnbe</code>	$\sim$ CF & $\sim$ ZF	Above
Unsigned	<code>setnb / setae</code>	$\sim$ CF	Above or equal
Signed	<code>sets</code>	SF	Negative
Signed	<code>setns</code>	$\sim$ SF	Nonnegative
Signed	<code>setl / setnge</code>	SF ^ OF	Less than
Signed	<code>setle / setng</code>	(SF ^ OF) ZF	Less than or equal
Signed	<code>setg / setnle</code>	$\sim$ (SF ^ OF) & $\sim$ ZF	Greater than
Signed	<code>setge / setnl</code>	$\sim$ (SF ^ OF)	Greater than or equal

Table: Set instructions