The basics of logic design: Sequential logic

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Announcements

Combinational logic
- Decoders
- Multiplexers

PA6 Demo code: directMapped read logic

Sequential logic
- SR latch
- SRAM cell

Announcements

Class session plan

- Thursday, 4/27: Diving deeper: Digital logic. (CS:APP Chapter 4.2) (Recommended reading: Patterson & Hennessy, Computer organization and design, appendix on "The Basics of Logic Design." Available online via Rutgers Libraries)
- Monday, 5/1: Survey of advanced topics in computer architecture.
- Thursday, 5/4: 8:00-11:00 AM, Hill 114, closed book, closed notes, no electronic devices, no calculator final exam.

Combinational vs. sequential logic

Combinational logic

- No internal state nor memory
- Output depends entirely on input
- Examples: NOT, AND, NAND, OR, NOR, XOR, XNOR gates, decoders, multiplexers.

Sequential logic

- Has internal state (memory)
- Output depends on the inputs and also internal state
- Examples: latches, flip-flops, Mealy and Moore machines, registers, pipelines, SRAMs.

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Decoders

Takes n-bit input, uses it as an index to enable exactly one of 2^n outputs

Internal design of 1:2 decoder

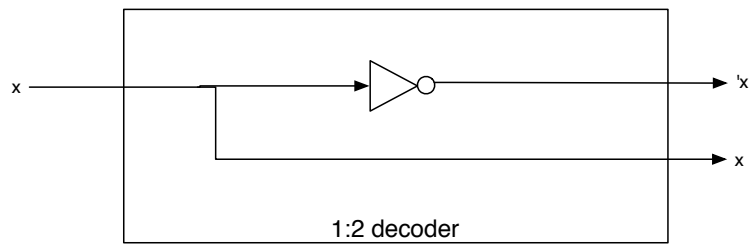


Figure: Source: Mano & Kime

Decoders

Hierarchical design of decoder (2:4 decoder)

Takes n-bit input, uses it as an index to enable exactly one of 2^n outputs

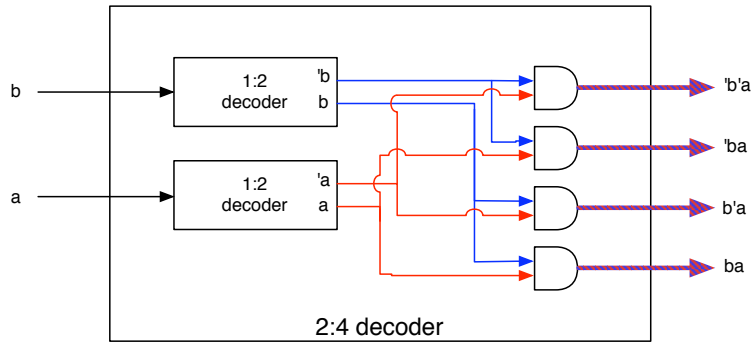


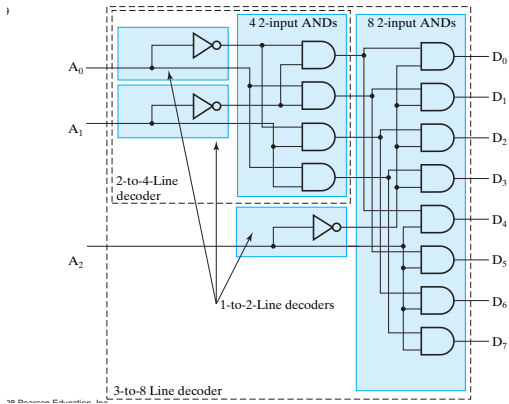
Figure: Source: Mano & Kime

Decoders

Takes n-bit input, uses it as an index to enable exactly one of 2^n outputs

Decoder (3:8)

Hierarchical design: use small decoders to build bigger decoder



Note: A_2 "selects" whether the 2-to-4 line decoder is active in the top half (A_2=0) or the bottom (A_2=1)

Figure: Source: Mano & Kime

Multiplexers

Using n-bit selector input, select among one of 2^n choices

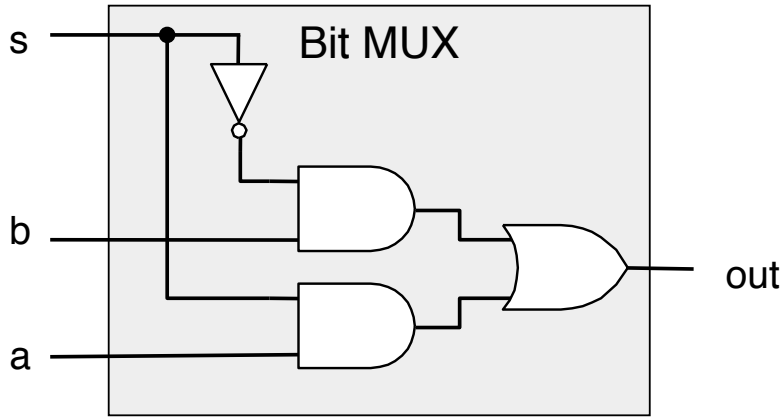


Figure: Source: CS:APP

Multiplexers

Using n-bit selector input, select among one of 2^n choices

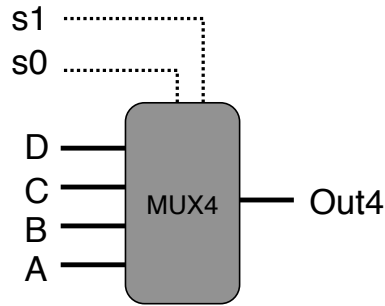


Figure: Source: CS:APP

Multiplexers

Using n-bit selector input, select among one of 2^n choices

Internal mux organization

3-26

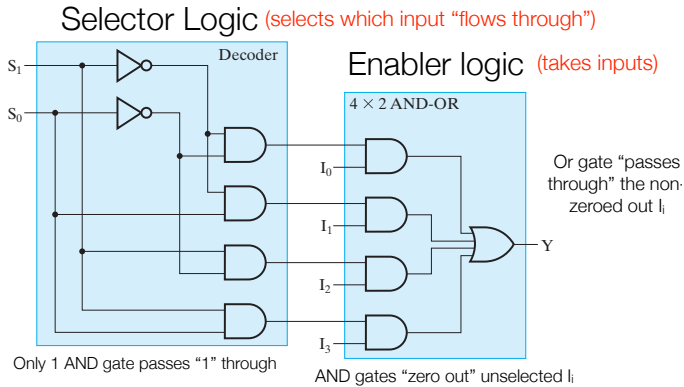


Figure: Source: Mano & Kime

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directMapped read logic

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Sequential logic

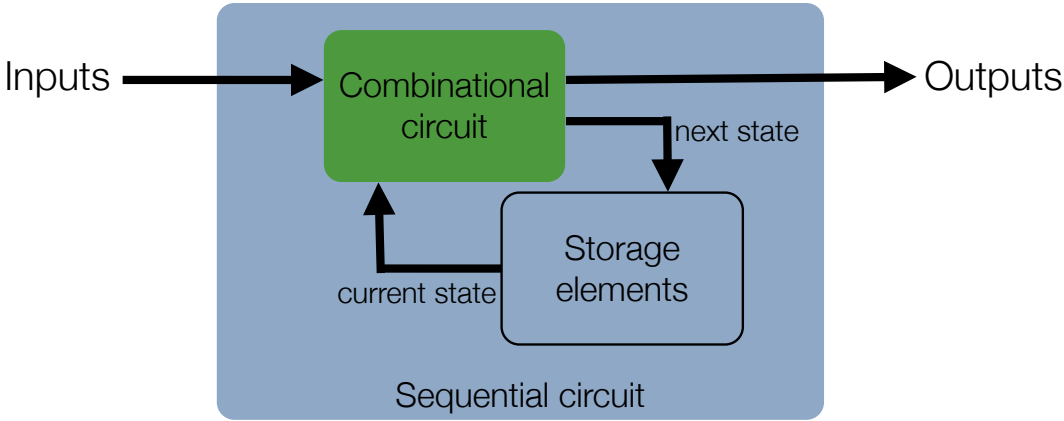


Figure: Source: Mano & Kime

The simplest sequential logic element: The set/reset (SR) latch

SR latch

- Latch constructed of cross-coupled NOR gates

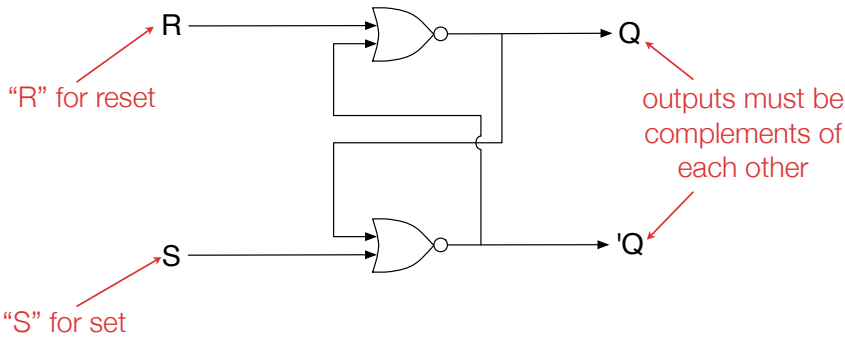
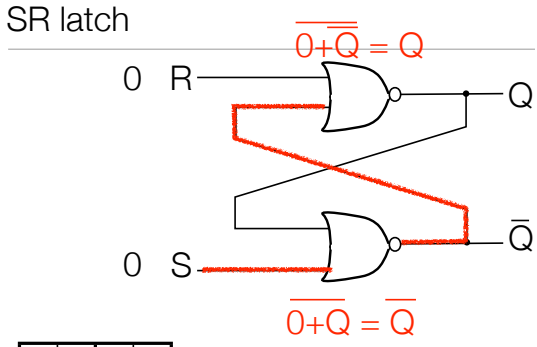


Figure: Source: Mano & Kime

The simplest sequential logic element: The set/reset (SR) latch



R	S	Q	$\overline{Q}$
0	0	Q	$\overline{Q}$
0	1	1	0
1	0	0	1
1	1		

Hold previous value

Figure: Source: Mano & Kime

6 transistor SRAM cell

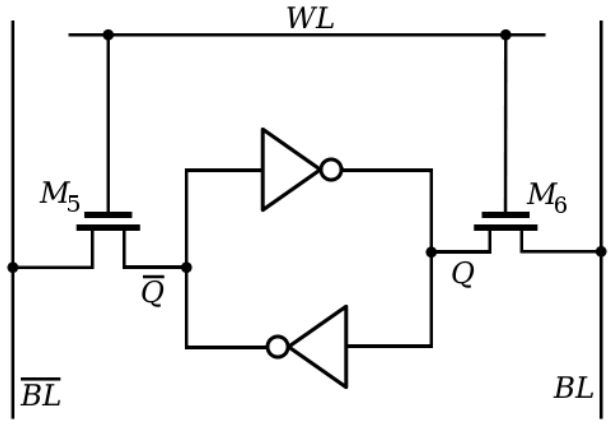
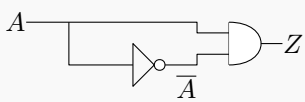


Figure: Source: Wikimedia

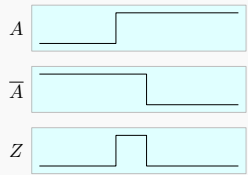
Asynchronous / Synchronous circuits

Timing

Circuit:



Voltages over time:



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